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Interfacing with a capacitance based strain sensor for use in CNC milling applications

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INTERFACING WITH A CAPACITANCE BASED STRAIN SENSOR FOR USE IN CNC MILLING APPLICATIONS

BY

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THESIS

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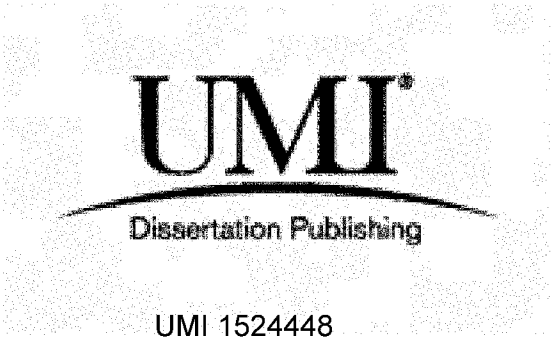

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DEDICATION

To Mom and Dad

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ABSTRACT

INTERFACING WITH A CAPACITANCE BASED STRAIN SENSOR FOR USE IN CNC MILLLING APPPLICATIONS

By

Christopher Dean

University of New Hampshire, September, 2013

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"Smart machining" provides feedback to the machine in an attempt to avoid pushing the cutting tool beyond its capability or lifetime, potentially ruining the tool or workpiece. This thesis details the process of designing a circuit board for communication with a capacitance-based wireless strain sensor to achieve a target strain resolution of $10\mu\epsilon$, at a target measurement rate of 100 kHz. The sensor resonates at a particular frequency, which varies as a function of strain on the tool. The strain is calculated as a function of the change in the resonant frequency. The results of this research are presented in terms of the effective sampling rate based on the number of samples to average in order to obtain a measurement, where based on the noise in the measurement, 280 samples must be averaged in order to obtain a strain measurement. These results demonstrate the successful concept of wireless strain measurement with a capacitance-based sensor.

CHAPTER 1

Introduction

1.1 Introduction

A Computer Numerically Controlled (CNC) milling machine uses rotary cutting tools that spin up to tens of thousands of revolutions per minute (RPM). The purpose is to remove material in a precise, controlled manner to create potentially complex designs, and do so repeatedly and reliably. The University of New Hampshire has a CNC machine in the Design and Manufacturing Lab, shown in Figure 1.1.

Figure 1.1: CNC Machine inside UNH Design Manufacturing Lab

The CNC machine shown removes material at a spindle rate up to 7,500 RPM with a tolerance of 0.0001 inches for each cut. Figure 1.2 shows an example of a part produced by a CNC machine (right) from raw stock (left).

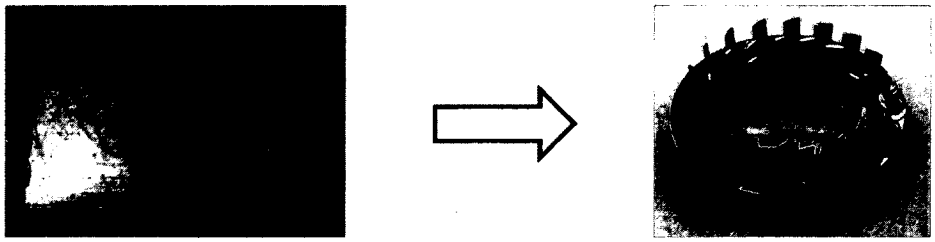


Figure 1.2: Raw Stock and Milled Workpiece

In milling applications, machine tool wear has a major effect on both cost and quality of machined parts. Currently, most milling operations are performed open loop, meaning there is no feedback used to control the process, which can lead to improper feed rates or spindle speeds. If a tool is not changed until after it has become dull or chipped, the workpiece can be damaged, resulting in increased costs to remanufacture the part. Changing a tool too early will prevent damage to the workpiece, but will unnecessarily raise cost as well. Research has shown that tool failure is responsible for approximately 20% of machine downtime, and implementing a suitable sensor feedback control system can prevent a majority of these failures [1].

"Smart machining" is a term used to describe the process of adding sensors to the machining environment to provide the feedback necessary to control the process so as to decrease machine downtime. While several sensors have been developed for controlling the machine process, they all have drawbacks that do not exist for the approach used in this research.

One possible approach employs microphones to extract the frequency content related to chatter vibrations [2]. Chatter, or self-excited vibrations, is the vibration between the tool and workpiece that causes poor workpiece surface quality and increases cutting forces. Higher cutting forces lead to accelerated tool wear and/or breakage. The microphone monitors the acoustic spectrum inside the machining environment and provides feedback to limit chatter. The use of the microphone is non-intrusive to the machining process, but is not capable of providing sufficient information regarding strain on the tool to control the process.

Another design is a machine-tool sensor that uses traditional strain gages inside a custom tool holder and transmits strain data to a computer via Bluetooth, shown in Figure 1.3. The strain cannot be measured directly on the tool because strain gages require wires that lead to a

measurement device, and the rotation of the tool would result in the wire wrapping around the tool. Since the measurement cannot be taken directly on the tool, the strain data is measured inside the custom tool holder some distance away from the cutting tool, and the forces of the tool are approximated from those measurements.

A major drawback to using the custom tool holder is that it changes the compliance of the machining system. The compliance of the milling process is altered because of the additional mass and length associated with the tool holder, which affects the machine dynamics. For the same force applied to a longer moment arm, the strain at the base of the arm increases. The increase in force prevents the machine from running at maximum efficiency, ultimately decreasing manufacturing efficiency and increasing cost. The custom tool holder system also requires periodic charging of the battery, and costs between $1,000 and $2,000.

A Kistler force dynamometer, pictured in Figure 1.4, is a device that mounts inside the CNC machine, with the workpiece mounted on top of the dynamometer. It contains a three-axis load cell capable of measuring a force in all three spatial dimensions. The dynamometer adds additional compliance to the machining system due to the nature of the force measurement, because in order to measure a force the dynamometer must displace a certain amount. That larger displacement for an applied force will result in a larger displacement of the workpiece, which will in turn negatively affect the quality of the workpiece. The Kistler force dynamometer is also expensive, costing between $30,000 and $45,000.

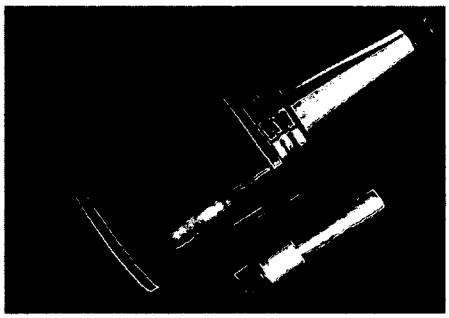


Figure 1.3: Custom Tool Holder for Strain Gage Measurement and Bluetooth Data Transmission

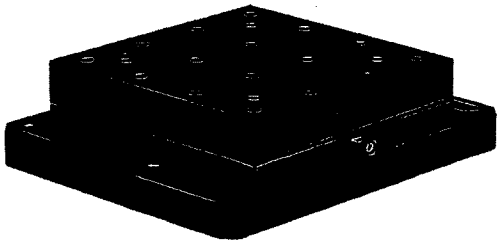


Figure 1.4: Kistler Force Dynamometer

1.2 Background

Currently, the most commonly used strain gage is a metallic foil pattern attached to a specimen by adhesive. As the tool is strained, the deformation of the tool changes the shape of the metal foil, which results in a change in its electrical resistance. The approach applied in this thesis uses a similar concept, except that the sensor is a strain-sensitive capacitor. The strain on the tool causes the capacitor to change its dimensions, which changes the capacitance. Figure 1.5 and Figure 1.6 picture a resistive strain gage and an interdigitated capacitor that was used in the work presented here. The resistive strain gage and interdigitated capacitor appear similar, but the resistive strain gage is a single piece of metallic foil, whereas the interdigitated capacitor sensor must have spacing between two sets of fingers for a capacitance to exist. Both sensors respond to strain with a change in the dimensions of the device. The resistive sensor responds to a strain with a change in the resistance of the metallic foil, while the interdigitated capacitor responds with a change in the capacitance.

Figure 1.5: Resistive Strain Gage [3]

Figure 1.6: Interdigitated Capacitor

An interdigitated capacitor is a good choice for strain-sensitive applications, because it allows for strain measurements without a direct, wired connection. The interdigitated fingers stretching across the area of interest resemble that of a typical resistive strain gage. Similar to a resistive strain gage, when the interdigitated capacitor is adhered to a specimen, the strain on the specimen will propagate through to the capacitor, changing the dimensions of the fingers and finger spacing. The capacitance of an interdigitated capacitor (IDC) is a function of the area between each finger. When the capacitor is strained, the area between fingers will change, causing a change in capacitance. A layer of polyimide on each side provides insulation for the IDC sensor. An example of an IDC sensor used in this research is shown in Figure 1.7. Refer to Appendix A for more information about the IDC sensor.

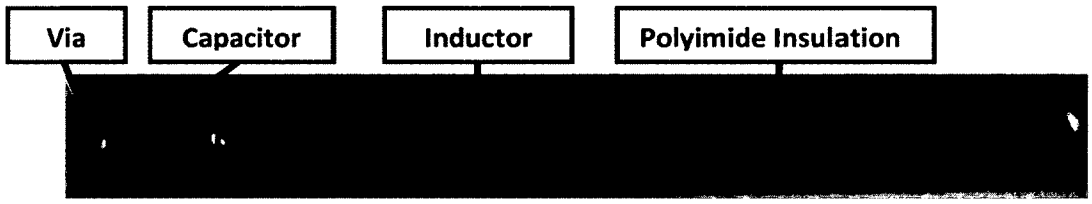


Figure 1.7: Example of IDC Sensor used in this Research

The steel specimens used in this thesis were not actual cutting tools, but 0.5" high strength steel rods. The only difference between a CNC cutting tool and these specimens is that the slug is not machined into a cutting tool, which allows the slug to be more readily tested in various compression or tension configurations. Figure 1.8 shows an IDC sensor adhered to a steel slug with Kapton tape applied to the steel behind the sensor to reduce electrical losses introduced by the steel by providing another layer of insulation.

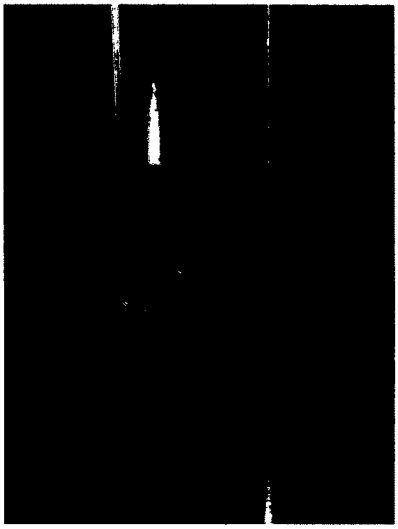


Figure 1.8: IDC Sensor on 0.5" Steel Slug with Kapton Tape Backing Material

The capacitance of the sensor is a function of the strain on the machine tool. In order to measure the capacitance, an inductor is added in series to form a resonant circuit, where the resonant frequency is dependent on the value of both the inductor and capacitor. For the sensor used in this research, the inductor is an insulated conductive loop that wraps around the machine tool and is terminated by the capacitor. The value of the inductor in this application is assumed constant, resulting in a resonant frequency for the inductor-capacitor circuit that will change as a function of the sensor capacitance. Since the value of the capacitor responds to strain, the resonant frequency is a function of the strain on the machine tool. Measuring the resonant frequency without direct contact with the machine tool is a primary topic of this thesis.

The next section provides an overview of resonance and the factors that affect it, as it is the basis for the measurement system used in this thesis.

1.2.1 Resonance

Resonance in an electronic circuit occurs at the frequency where the reactances of the impedance caused by both the capacitive and inductive elements in the circuit are of equal

magnitude and opposite phase, i.e. the two are 180° out of phase. The reactance of an ideal capacitor and inductor respectively are:

$$X_c = \frac{1}{2\pi fC} \tag{1.1}$$

and

$$X_L = 2\pi fL \tag{1.2}$$

where X_C is the reactance of the capacitor, C is the capacitance, X_L is the reactance of the inductor, L is the inductance, and f is the frequency of the system. At low frequencies, the reactance is dominated by the capacitance, and at high frequencies, the reactance is dominated by the inductance as shown in Figure 1.9 and Figure 1.10.

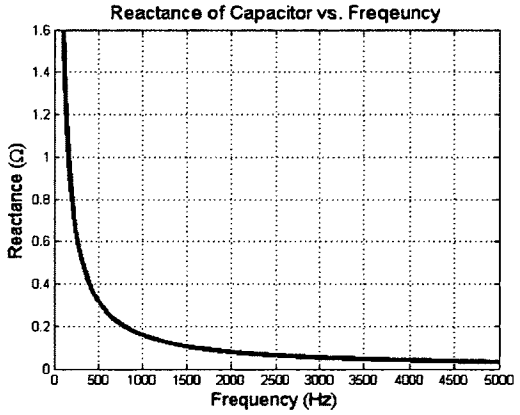


Figure 1.9: Reactance of a Capacitor vs. Frequency

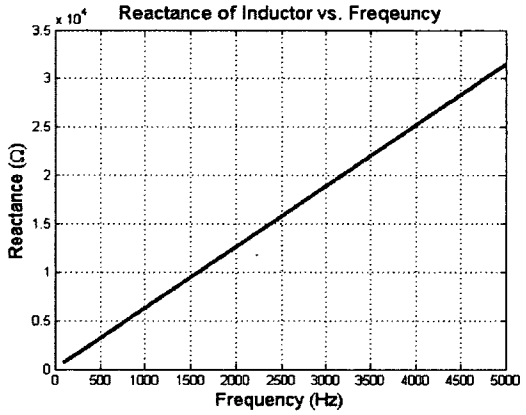


Figure 1.10: Reactance of an Inductor vs. Frequency

When the reactance of the capacitor and inductor are equal:

$$\frac{1}{2\pi fC} = 2\pi fL$$

$$(2\pi f)^2 LC = 1 \tag{1.3}$$

$$2\pi f = \frac{1}{\sqrt{LC}}$$

Finally, the resonant frequency is:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{1.4}$$

The capacitor and inductor can be in either a series or parallel configuration. If a series circuit is used, the resonance is indicative of an impedance minimum, while in a parallel circuit, resonance corresponds to an impedance maximum. The focus of this discussion will be on the series resonant circuit, as the sensor studied behaves as a series inductor-capacitor resonant circuit.

A circuit that consists of pure inductance and pure capacitance is not achievable in the lab due to the losses introduced from non-ideal components. The model of a non-ideal inductor includes series resistance, representing the DC resistance of the wire, and a parallel capacitor representing the capacitance between each turn of the inductor. The model of a non-ideal inductor is shown in Figure 1.11, where L represents the inductance, R_P represents the parasitic resistance introduced by the DC wire resistance, and C_P represents the parasitic capacitance introduced by the capacitance between wire turns.

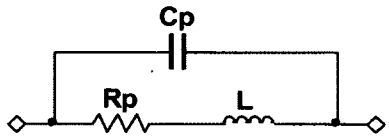


Figure 1.11: Model of Non-Ideal Inductor

A non-ideal capacitor, modeled in Figure 1.12, has parasitic series resistance and parasitic series inductance. The parasitic resistance, R_P, includes the leakage current resistance of the capacitor as well as the lead resistance that forms the physical connection to the circuit. The parasitic inductance, L_P, is the inductance from the leads at the physical connection to the circuit.

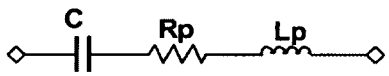


Figure 1.12: Model of Non-Ideal Capacitor

The inductor in the sensor does not complete one full turn, and therefore the parasitic capacitance of the inductor is neglected in this case, as it will be negligibly small. Lumping the

parasitic resistance of each component together, and combining the parasitic inductance of the capacitor with the nominal inductance of the sensor, the model of the LC sensor is shown in Figure 1.13.

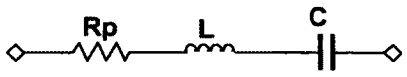


Figure 1.13: Model of IDC Sensor

A resonant circuit is modeled in Figure 1.14 with a discrete capacitor, discrete inductor, and the parasitic resistance in series.

The frequency response of any resonant circuit can be measured by varying the frequency of the AC voltage source V1 and plotting the current through the loop as a function of frequency. The simulated voltage source V1 holds a constant output voltage of 1 volt for all frequencies. The current through the loop, as governed by Ohm's Law, is inversely proportional to the magnitude of the complex impedance in the circuit. The current through the loop increases at resonance due to lower overall impedance in the circuit, because the reactance of the inductor and capacitor cancel. The values for the components in Figure 1.14 were chosen to be similar to values for the IDC sensor, but are not exact and are used for example purposes.

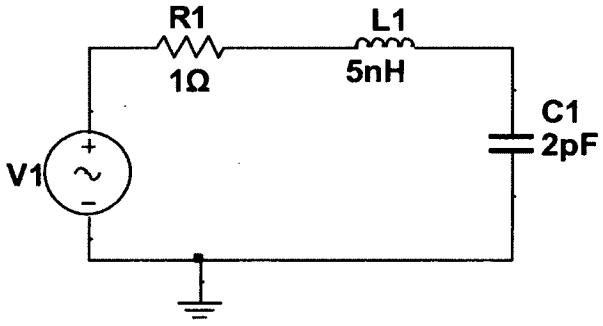


Figure 1.14: Simple Series Resonant Circuit

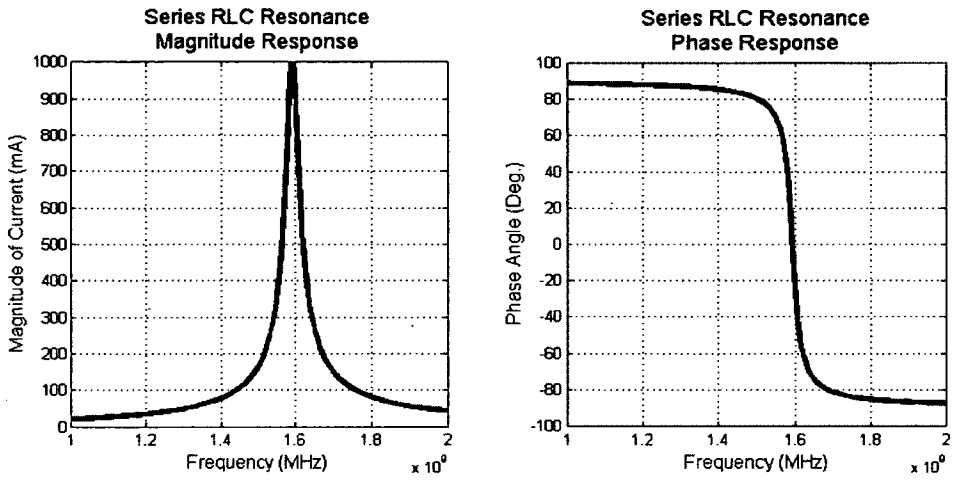


Figure 1.15: Series Resonance Response

A commonly used metric used to characterize resonant circuits is the Q factor, also referred to as simply the Q. The Q factor is defined as [4]:

$$Q = \frac{f_{res}}{f_{bw}} \tag{1.5}$$

where f_{bw} is the -3dB bandwidth. The Q factor is inversely related to changes in the bandwidth for the same resonant frequency. A higher Q factor leads to a faster roll-off and a more pronounced resonance peak. The resonant frequency can still be determined for lower Q values, but in the operational environment, which includes noise, a lower Q makes high-resolution measurements challenging.

The value of the resistor in Figure 1.14 affects the Q factor, as demonstrated in Figure 1.16, where an increase in resistance by a factor of five decreases the Q by a factor of five. The resistance is the parasitic resistance of both the inductor and capacitor, which will vary with the design of the sensor inductor and capacitor. A high Q factor is desirable for this application, where identifying the resonant frequency is the goal.

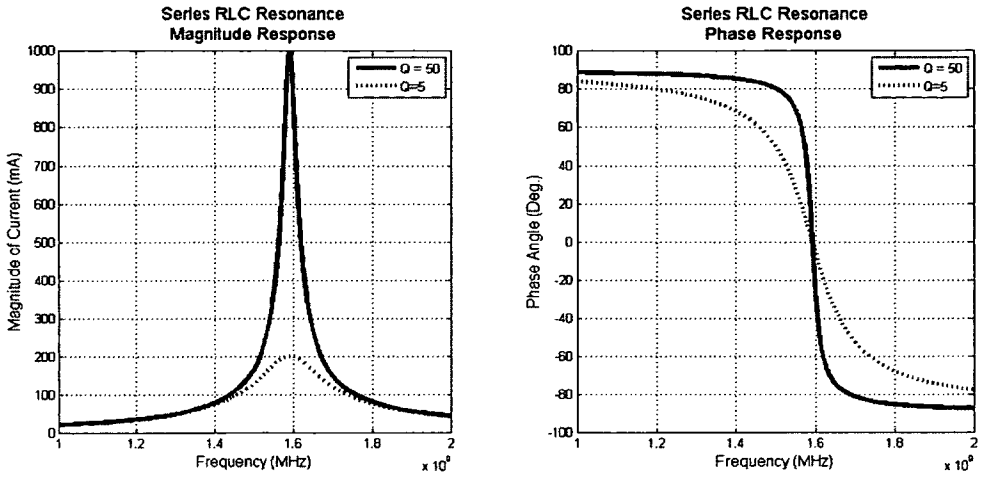


Figure 1.16: Series RLC Response with Lower Q Factor

The actual resonant frequency of each IDC sensor is dependent on the dimensions of the capacitor sensor and inductor loop. Multiple sensor designs have been tested throughout this research, and have been experimentally determined to resonate within the range of 1 GHz to 2 GHz.

1.2.2 Strain Response

The IDC sensor is directly attached to the tool, and so any strain experienced by the tool will be experienced by the capacitor as well. Strain is a unit-less quantity, defined as the ratio of total deformation to the initial length [5]:

$$\epsilon = \frac{\Delta L}{L} \qquad (1.6)$$

It is worth noting that the symbol used for strain in mechanical engineering, ϵ, is the same symbol used for relative permittivity in electrical engineering, and both are discussed in this thesis, but are not used simultaneously in any equations or calculations.

The goal for the work presented in this thesis is to measure strain with resolution to one part in 10^5, which matches or exceeds the force measurement resolution of the Kistler force dynamometer. As noted above, the IDC sensor consists of a strain-sensitive capacitor and

inductor loop. The inductor exists to allow the sensor to resonate, and does not change with strain. Therefore, in the sensor model, the interdigitated capacitor is modeled as a variable capacitor and the inductor value is held constant, as shown in Figure 1.17. The capacitance of the sensor will change as a function of strain and the initial capacitance:

$$C = C_0(1 + \epsilon) \tag{1.7}$$

The resultant resonant frequency will change as a function of C:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{1.8}$$

where f_{res} is a function of strain because C is a function of strain, as seen in Equation (1.7).

$$\left.\begin{aligned} \Delta f_{res} &= f_{res} - f_{res_0} \\ \Delta f_{res} &= \frac{1}{2\pi\sqrt{LC}} - \frac{1}{2\pi\sqrt{LC_0}} \\ \Delta f_{res} &= f_{res0}\left(\frac{1}{\sqrt{1+\epsilon}} - 1\right) \end{aligned}\right\} \tag{1.9}$$

The Taylor series approximation of the change in resonance for $\epsilon \ll 1$ is:

$$\frac{1}{\sqrt{1+\epsilon}} = 1 - \frac{\epsilon}{2} + \frac{3\epsilon^2}{8} - \cdots \tag{1.10}$$

where a first order approximation is

$$\Delta f_{res} = f_{res0}\left(-\frac{\epsilon}{2}\right) \tag{1.11}$$

The resonance shift in the model is a function of the capacitance change as seen in Figure 1.18.

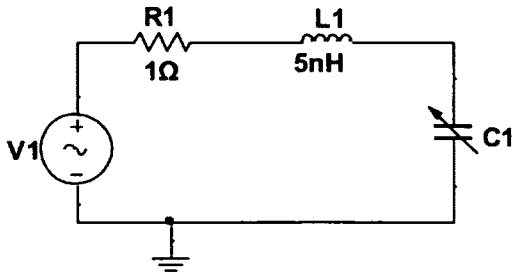


Figure 1.17: Model Resonant Circuit with Variable Capacitor

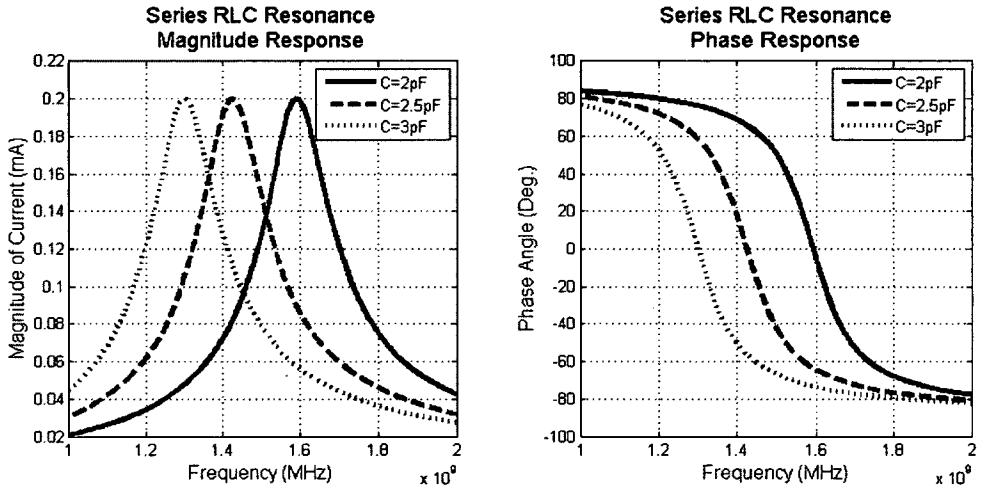


Figure 1.18:Shift in Resonance as Capacitance Changes

Figure 1.19 shows the change in the resonant frequency for different values of capacitance experiencing the same strain of one part in 10^5. The plot shows the change in resonant frequency in response to strain on the left axis, and the modeled absolute resonant frequency according to Equation (1.4) on the right axis. A smaller capacitance will yield a higher absolute resonant frequency and a larger change in resonance.

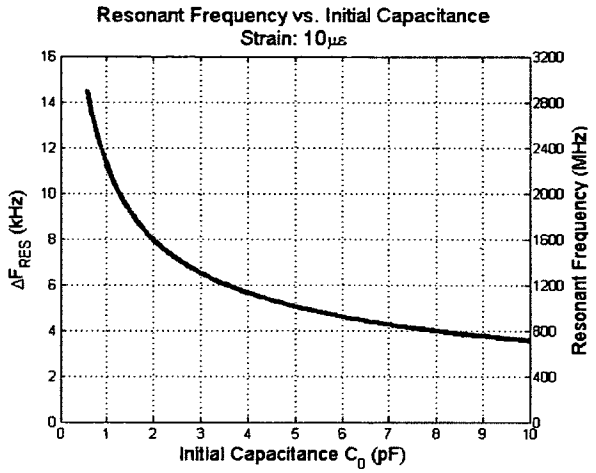


Figure 1.19: Resonant Frequency Response to Capacitor Strain

1.2.3 Measuring Resonant Frequency through Inductive Coupling

As described above, the strain on the tool can be determined from the resonant frequency of the IDC sensor. The resonant frequency itself does not provide strain information, as the system will naturally resonate at a particular frequency. It is the change in the resonant frequency that corresponds to the strain on the tool.

To measure the resonant frequency of the IDC sensor without direct electric contact with it, the sensor is placed inside a larger stationary loop as shown in Figure 1.20 and Figure 1.21. The loop is fabricated on a printed circuit board (PCB) as shown in Figure 1.20, and is referred to as the probe loop throughout this thesis. A high frequency signal is passed through the probe loop and the electromagnetic fields generated couple with the sensor loop, inducing currents on the IDC sensor. The currents through the IDC sensor will cause it to resonate, and the effect of resonance will couple onto the probe loop, and is measured at the output terminal of the probe loop.

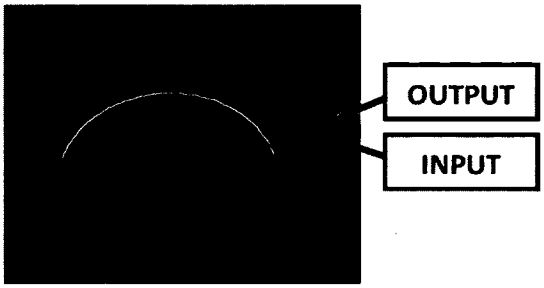


Figure 1.20: Probe Loop

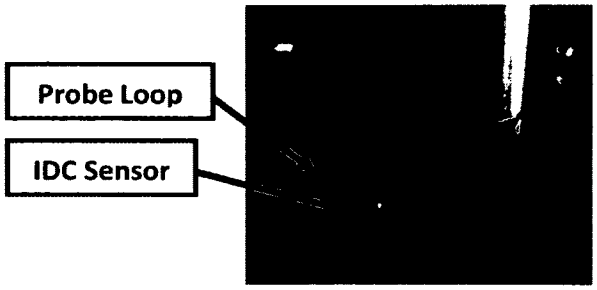


Figure 1.21: IDC sensor in Probe Loop

If the sensor circuit obeyed the well-defined equations for resonance, such as in the resonant circuit shown in Figure 1.17, without influence from external factors such as noise or dependence on position, the resonant frequency could be determined without any limit on resolution. However, in the operational environment, the IDC sensor is sensitive to displacement with respect to the probe loop as well as strain, and noise obscures the resolvable value. The design of a circuit with the lowest possible noise to achieve the target resolution of one part in 10^5 is the focus of this thesis.

1.3 Advantage of Using a Capacitance Based Strain Sensor

The major potential advantage associated with using a capacitance-based sensor as opposed to a resistive-based sensor in a machining application is the ability to measure strain without a physical or direct electrical connection, and therefore does not introduce compliance issues to the system. The tool will be able to operate as it was designed, as opposed to operating with speed or feed rate limitations resulting from a force measurement system that introduces compliance as previously mentioned.

The sensor and detection system presented here has potential to be lower cost than previous smart machining solutions. Assuming the techniques developed in this research are proved successful, the relatively small additional costs introduced from employing this technique has the potential to change the industry, resulting in significant long-term savings for

manufacturers using CNC milling machines. The capacitive sensor will attach to the tool for the lifetime of the tool, as it is inexpensive enough to replace when replacing the tool.

1.4 Thesis Overview

The focus of this thesis is the design of a circuit used to measure changes in the resonant frequency with a target resolution of one part in 10^5, or 10 $\mu\epsilon$. The noise in the system plays a large part in the achievable resolution. The component selection, both active and passive, as well as component placement and printed circuit board layout play a key role in noise reduction. This thesis details a circuit designed for the lowest noise possible with available components.

Chapter 2 describes the circuit used to determine the changes in the resonant frequency by implementing a feedback loop . The external data acquisition device and the methods of fabrication of the circuit are also discussed.

The concept of noise in an electronic circuit is detailed in Chapter 3. Different types of noise, as well as noise in both the time and frequency domain are discussed. The impact of noise on each component is considered, and the circuit is modeled with noise injected according to each component.

Chapter 4 presents the measured data collected using the system described in this thesis. Testing consisted of both unstrained static and dynamic load ramp tests. The measurement system is designed for the lowest possible noise. The design includes the best noise performance devices available, with a PCB component layout designed for noise reduction. The final analysis presents the results in terms of the time required to perform a measurement at multiple resolutions.

Chapter 5 is the final discussion and conclusions from this research. It also contains ideas for future improvements to take this concept and bring it to the level needed to suit industry applications.

This thesis does not go into detail about the strain-sensing capabilities of the IDC sensor, but focuses on low noise circuit design. Refer to K. F. Shaughnessy [6] for a thesis from the mechanical engineer on this research, which details the analysis of the IDC sensor and its response to strain.

CHAPTER 2

Resonance Detection and Tracking Circuit

2.1 Introduction

The circuit implemented for resonant frequency measurement is an analog control loop circuit, capable of operating in both closed loop and open loop form. The normal operation of the circuit is closed loop, and is called the tracking mode. The open-loop mode is known as the diagnostic mode, which performs a wide bandwidth frequency sweep to identify the rough location and Q of the resonance. The closed-loop tracking mode then locks to a user-specified location on the frequency response, adjusting the system frequency in response to strain to maintain a locked state.

2.2 High Frequency Component Selection

In order to track the resonant frequency, the system must be capable of generating and measuring a high frequency signal. This section discusses the radio frequency (RF) components that generate the high frequency signal needed for the IDC sensor to resonate and the components required to measure the response of the IDC sensor.

To measure the frequency response of the IDC sensor, a signal that does not propagate through the probe loop is used as a reference to compare against. An RF splitter will split the RF power equally into two separate channels, allowing one channel to lead into the probe loop and the other channel to serve as the reference.

A voltage controlled oscillator (VCO) and an integrated circuit (IC) that can detect the relative magnitude and phase difference between two signals are well suited for this application. A VCO produces an RF output frequency proportional to an analog input voltage. The magnitude/phase detector IC responds to the difference in both the magnitude and phase between two RF signals, in this case the reference signal and the test signal. A block diagram of the entire RF circuit is shown in Figure 2.1. Appendix B contains detailed specifications of each component.

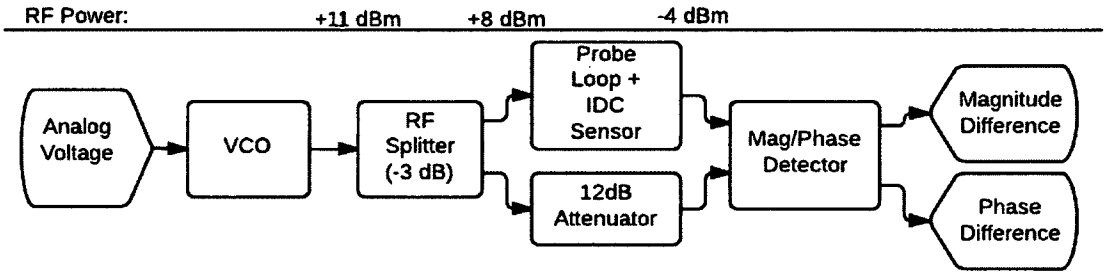


Figure 2.1: Block Diagram for IDC Sensor Resonance Measurement

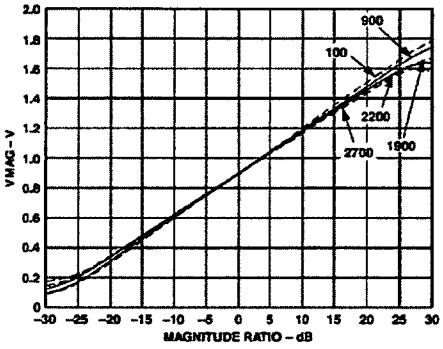
Different VCO's exhibit different characteristics including output frequency range, input tuning voltage range, output RF power, and noise. Consequently, the VCO has a significant impact on system performance. The ROS-2230 from MiniCircuits was chosen because it has an output frequency range of 1064 MHz to 1968 MHz, covering the resonant frequency range of most of the IDC sensors used in this research, for a tuning voltage between 0 V and 10 V. The output RF power is measured in terms of dBm, which is a power ratio in dB with respect to 1 mW. The output power of the ROS-2230 is +11 dBm.

Frequency pushing is the term used to describe the change in the output frequency of a VCO due to a change at the DC power supply of the VCO [7]. To minimize frequency pushing, a linear voltage regulator, a device that produces a constant DC voltage despite fluctuations caused by increased load current or input voltage, is used to supply the power to the VCO. The linear voltage regulators selected in this design are also discussed in detail in Appendix B.

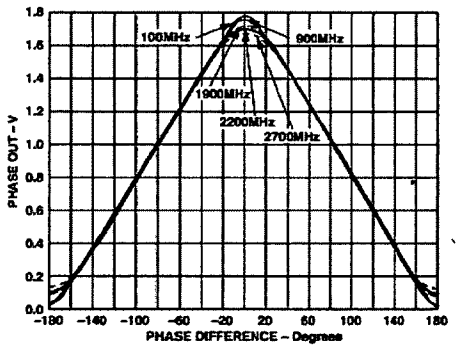
The magnitude/phase detector has two inputs, and two outputs. The output is an analog voltage between 0 V and 1.8 V, corresponding to the ratio of the difference in the magnitude and difference in angle of the phase between the two inputs. The analog voltage output channels are referred to as magnitude and phase in this thesis. The output of the magnitude channel represents the ratio of the two inputs from -30 dB to +30 dB over the 1.8 V range. The output is centered at 0.9V when the input signals are of equal amplitude. The output increases up to 1.8 V for +30 dB, and decreases to 0 V for -30 dB. The output sensitivity of each channel is shown in Table 2.1, and the transfer function from the datasheet is shown in Figure 2.2 [8].

Table 2.1: Magnitude/Phase Detector Output Sensitivity and Center Point

Output	Sensitivity	Center Point (0.9V)
Magnitude	30mV/dB	0dB Difference
Phase	10mV/Degree	90° Difference



TPC 1. Magnitude Output (VMAG) vs. Input Level Ratio (Gain) V_{INPA}/V_{INPB}, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, 2700 MHz, 25°C, P_{INPB} = –30 dBm, (Re: 50 Ω)



TPC 25. Phase Output (VPHS) vs. Input Phase Difference, Input Levels –30 dBm, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, Supply 5 V, 2700 MHz

Figure 2.2: Magnitude and Phase Transfer Function From the Magnitude/Phase Detector Device Datasheet

The phase comparator does not indicate if the phase difference is positive or negative, so the output value only contains the absolute value of the phase difference. The output of the phase channel is centered at 0.9 V for a phase difference of 90°. The output is inversely related to the phase difference, increasing to 1.8 V for 0° offset, and deceasing to 0 V when the signals are 180° out of phase.

The maximum power of a RF signal that the magnitude/phase detector can accomodate is 0 dBm, and the output of the VCO used in this design is approximately +11 dBm. This required the use of attenuators, placed after the splitter, to reduce the signals to an acceptable level. The IDC sensor and probe loop coupled system was experimentally determined to attenuate approximately 12 dB of the signal by adjusting the attenuation on both lines until the magnitude output of the magnitude/phase detector read 0.9 V. A 12 dB attenuator after the RF splitter on the reference line provides 15 dB of combined attenuation from the RF splitter and in-line attenuator, for a power level of -4 dBm at the magnitude/phase detector input. An absolute power level of -4 dBm is close to the maximum input power of the device, but the signal will only decrease, as the signal cannot be amplified by the passive circuit. The design allows for the RF power reaching the probe loop that couples with the IDC sensor to be as large as possible with the components used. It also reduces the number of components along the RF transmission line.

2.3 Diagnostic Mode Operation

The circuit operation in diagnostic mode, where the circuit runs open loop to sweep a broad range of frequencies, is described in this section. The circuit measures the changes in magnitude and phase of the probe loop signal with respect to an unperturbed reference signal, as the input frequency sweeps from 1 GHz to 2 GHz. The frequency is calculated from the measured VCO tuning voltage and the VCO's specified sensitivity from the datasheet. The output frequency was confirmed in the lab with a spectrum analyzer for the same discrete points shown in the datasheet. Figure 2.3 shows the output frequency as a function of the input, as stated in the device datasheet [9], and is not a plot of measured data from the specific VCO used in the experiments for this research.

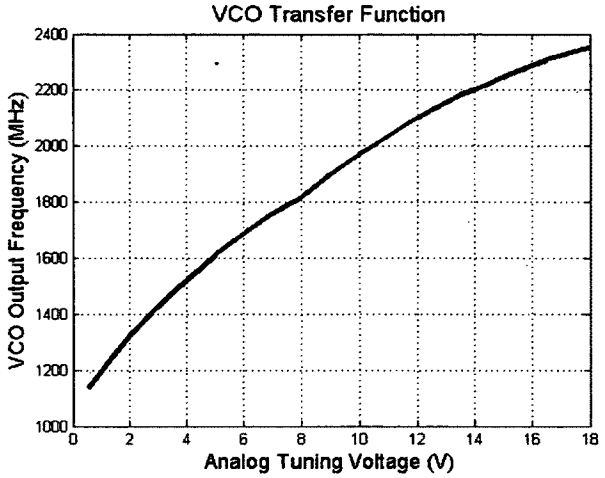


Figure 2.3: VCO Tuning Sensitivity

The hardware is controlled through an external data acquisition device (DAQ) with a digital-to-analog converter (DAC) and analog-to-digital converter (ADC). The device interfaces with LabVIEW software and sends a ramp signal from the external DAC to the VCO tuning voltage pin to sweep the VCO output frequency. The start and stop voltage, as well as the total number of points in the ramp, are all programmable. As the frequency output sweeps, the signal propagates through the reference and test transmission lines. For each point in the ramp, the external ADC records one sample of the magnitude and phase output from the magnitude/phase detector, as well as the VCO tuning voltage. Each sample from the magnitude/phase detector is then plotted against the calculated frequency output of the VCO for each point in the ramp. Figure 2.4 is an example of the response from the IDC sensor captured by the magnitude/phase detector, plotted against frequency output of the VCO. The RF section on the fabricated circuit is shown with labels in Figure 2.5. The schematic of the circuit is shown in Appendix D.

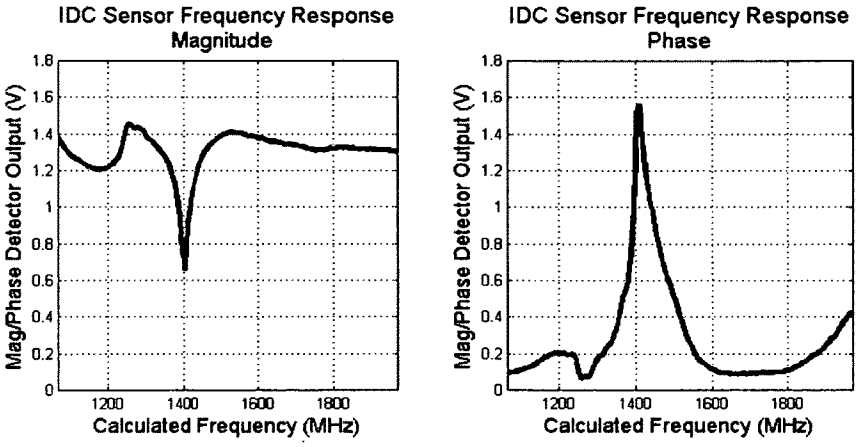


Figure 2.4: An Example of an IDC Sensor Frequency Response

Figure 2.5: Fabricated RF Section of Circuit

2.4 Tracking Mode Theory of Operation

The change in resonant frequency contains the strain information, and tracking the changes closely is necessary for high-resolution strain measurements. The closed-loop tracking circuit measures the small variations in resonant frequency in response to strain, and records the result with the external ADC. The closed-loop control circuit provides much greater resolution to measure the variation in resonant frequency in response to strain than the open-loop circuit by filtering out the noise inherent in the system.

The magnitude and phase response analog output voltages of the magnitude/phase detector both have a near-linear region within the resonant frequency range. The magnitude response is nearly linear for both a positive and negative slope between approximately 1350 MHz and 1450 MHz, with the slope changing from negative to positive at 1400 MHz, as

highlighted by the thick line in Figure 2.6. Similarly, the phase response is nearly linear from approximately 1390 MHz to 1410 MHz for a positive slope, and from 1410 MHz to 1500 MHz for a negative slope.

If the VCO is held constant at a point that falls along the near-linear region of the output, the magnitude/phase detector output is constant, assuming no external factors such as a strain or noise exist. The output of the magnitude/phase detector will increase or decrease according to the slope in response to shifts in the resonant frequency.

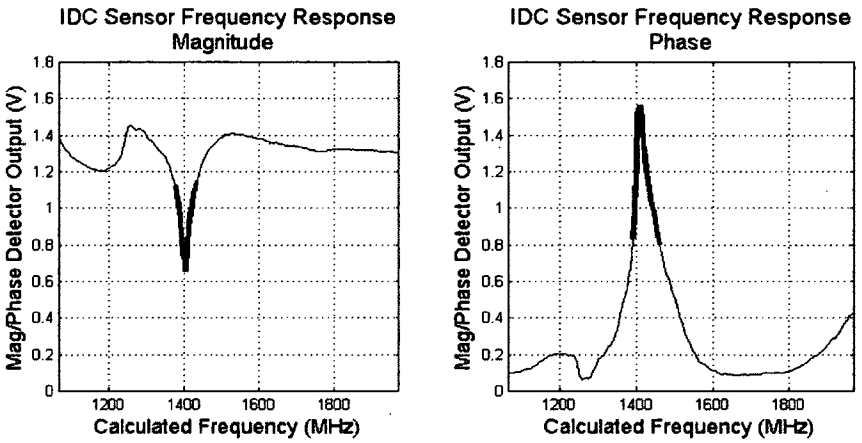


Figure 2.6: Highlighted Linear Region of Resonance Response

The circuit works by holding a fixed output of the magnitude/phase detector and adjusting the VCO input voltage to compensate for the resonance shift due to strain. The user selects the location on the resonance for the controller to lock on to, which is referred to as the control point. Figure 2.7 shows an example of the magnitude response with a selected control point, where V_{BIAS} is the input voltage to the VCO, and V_{HOLD} is the value of the magnitude/phase detector to hold constant. As the resonance shifts, the output of the magnitude/phase detector will increase or decrease depending on both the polarity of the slope and whether the resonant frequency is increasing or decreasing.

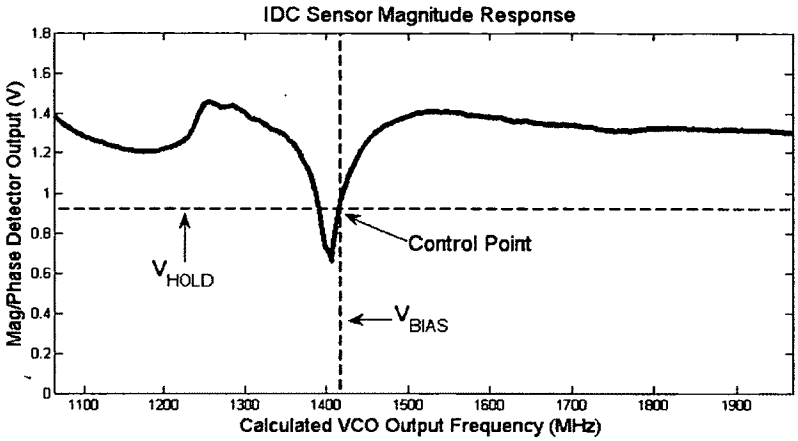


Figure 2.7: Control Point of Magnitude/Phase Detector Output for Fixed VCO Input

A shift in the resonance toward a higher frequency due to strain on the machine tool is shown in Figure 2.8, illustrated as 40 MHz for clarity. If the resonance shifts to the right, increasing in frequency, and the control point is on the positive slope, the magnitude/phase detector output will decrease. A change in the magnitude/phase detector output voltage is shown close-up in Figure 2.9, where the shifted response is 10 mV lower than the initial response, where the control point was c7hosen. To maintain the desired control point, the VCO output frequency must increase by approximately 800 kHz to get the system back to the control point.

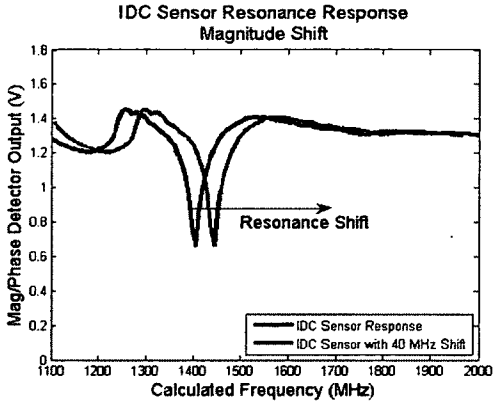


Figure 2.8: Large Scale Resonance Shift

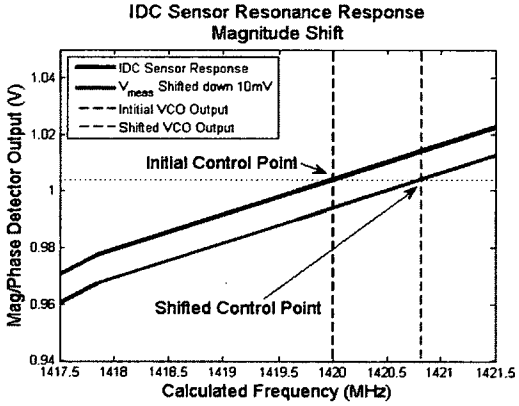


Figure 2.9: Small Scale Resonance Shift

Once the system has appropriately adjusted the VCO input voltage, the system will again operate at the desired control point. That is, if the magnitude/phase detector output increases

or decreases, the system will adjust the VCO output as a difference from this new VCO input voltage. Constantly adjusting the VCO input voltage reference point allows the system to respond to resonance shifts that would otherwise be greater than the bandwidth of the linear region of the response.

2.5 Tracking Circuit Design

When operating in the tracking mode, the software uses the external DAC to set the V_{BIAS} and V_{HOLD} points that were identified in resonance sweep from Figure 2.7. As stated above, the V_{BIAS} voltage is the initial, unstrained tuning voltage to the VCO, and V_{HOLD} is the voltage to lock to, adjusting the VCO to get the output of the magnitude/phase detector back to that voltage. The block diagram of the circuit is shown in Figure 2.10. Since the magnitude/phase detector has two outputs, but only one output can be used in the control feedback scenario implemented in this design, a switch exists between the magnitude/phase detector and controller, shown as SW1 on the block diagram, to select either the magnitude or phase output. There is another switch allowing the controller to operate on either a positive or a negative slope, shown as SW2. These two switches impact the selection of the control point, as the VCO input voltage and magnitude/phase detector output voltage depend on both. Once the switches and control point are properly set, the circuit can control the VCO. The output signal to the VCO contains the strain information, because the voltage to the VCO is adjusted in response to strain on the tool. The analog design is implemented in four op-amp stages, each discussed below.

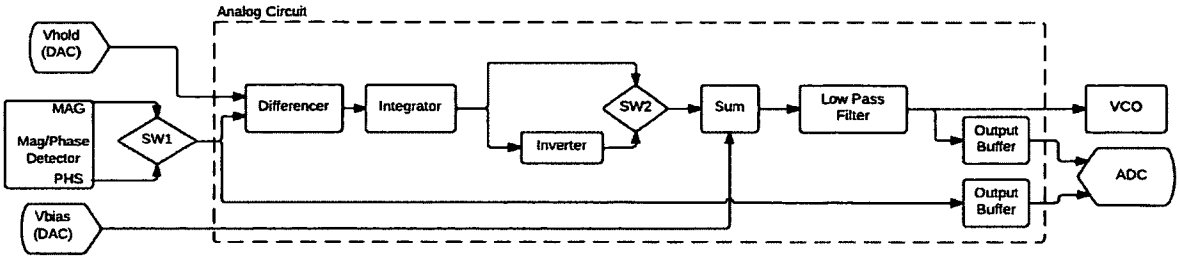


Figure 2.10: Analog Resonance Tracking Block Diagram

2.5.1 Difference Stage

The first stage is the difference between the measured magnitude/phase detector output voltage and the control point to hold. The measured output, referred to as V_{MEAS}, and the magnitude/phase detector control point, V_{HOLD}, are subtracted with an operational amplifier (op-amp) in a unity gain differencing amplifier configuration, shown in Figure 2.11.

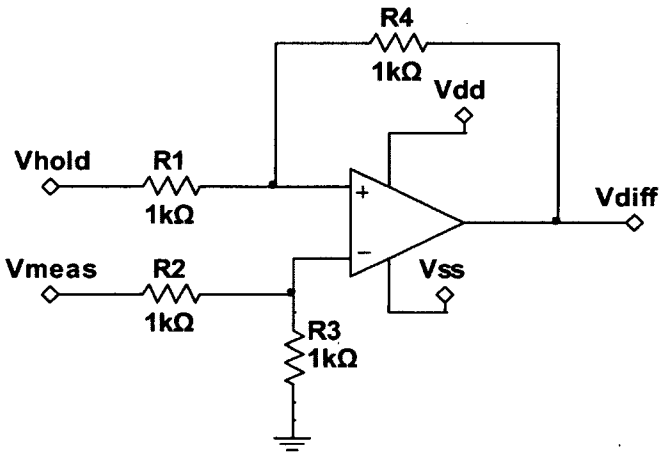


Figure 2.11: Unity Gain Differential Amplifter

$$V_{DIFF} = V_{HOLD} - V_{MEAS} \quad (2.1)$$

2.5.2 Integrator Stage

The second stage of the circuit integrates the difference produced by the differencing stage. The integrator circuit is an inverting amplifier, with the schematic shown in Figure 2.12 and governing equation below. The integrator will produce a ramp output for a constant, non-zero input, increasing or decreasing according to the polarity of the input voltage, until the op-amp

saturates and the output hits the supply rail. The output will hold constant if the input is zero. The rate of this

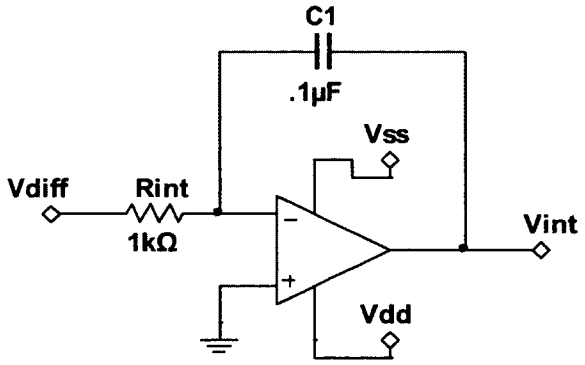


Figure 2.12: Integrator Circuit Schematic

ramp is determined by the time constant between the input resistor and feedback capacitor, which is the gain of the integrator. The output of an integrator circuit for a positive and negative step input is demonstrated for both a gain of 1 and gain of 0.5 in Figure 2.13.

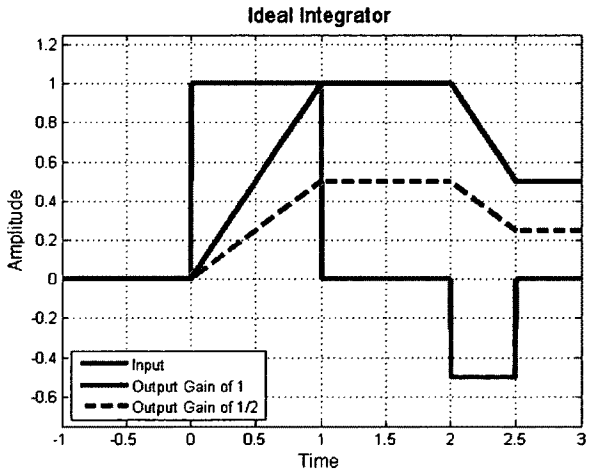


Figure 2.13: Simulated Output of Ideal Integrator

The voltage held at the output of the integrator will allow the VCO output to compensate for resonance shifts. When the difference between V_{HOLD} and V_{MEAS} is non-zero, the integrator output increases or decreases, adding to the VCO input voltage to drive the difference to zero. When the difference between V_{HOLD} and V_{MEAS} returns to zero, the integrator output holds that

output voltage. When the difference signal becomes non-zero again, the output of the integrator increases or decreases from that voltage.

$$V_{int} = -\frac{1}{RC}\int (V_{MEAS} - V_{HOLD}) \quad (2.2)$$

The integrator is also useful for reducing the noise in the system, as any zero-mean noise will integrate to zero over time. This is important in creating a circuit for low noise, high-resolution measurements.

2.5.3 Inverter Stage

Following the integrator is an inverter, which may be bypassed depending on the position of switch SW2 from the block diagram, which determines if the controller is working on a positive or negative slope. Positive slope control will employ the inverter, because the output of the integrator is inverted, so the signal will have to be inverted again before adding to the VCO_{BIAS} in the following stage. The circuit schematic for the inverter is shown in Figure 2.14, where SW2A and SW2B are latched together, and make up the switch SW2.

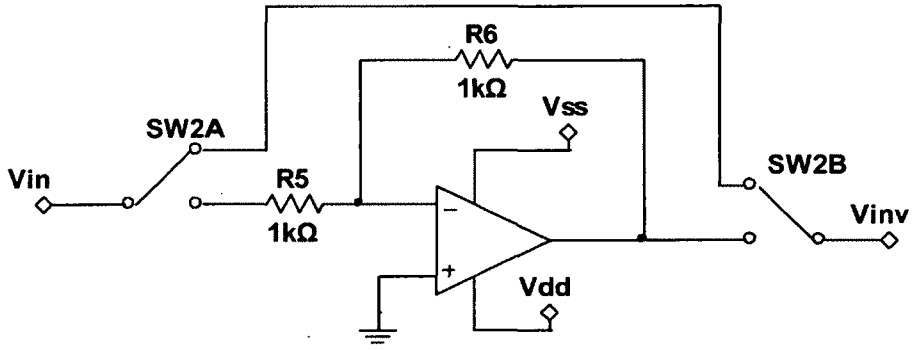


Figure 2.14: Inverter Circuit Schematic

2.5.4 Gain and Summation Stage

In order to generate a new tuning voltage for the VCO, a summing amplifier adds the result of the integrator with the VCO_{BIAS}. The output of the summing amplifier is a function of the feedback resistor and the input resistor for each input, as shown in the equation below. The

gain for the VCO_{BIAS} input is unity, with variable gain for the integrator output to allow for different resonance slopes. A potentiometer as the input resistor on the integrator output will allow for variable gain, while allowing the other to remain fixed at unity. A 50 $k\Omega$ potentiometer was selected given a 10 $k\Omega$ feedback resistor, to allow gain values down to 0.2 and an upper limit of 100. Figure 2.15 shows the circuit schematic of the summing amplifier, where the input V_{INT} is the voltage from the output of the integrator, inverted if necessary, and V_{BIAS} is the initial VCO input voltage based on the control point, generated by the external DAC. Equation (2.4) shows the simplified equation for V_{SUM}.

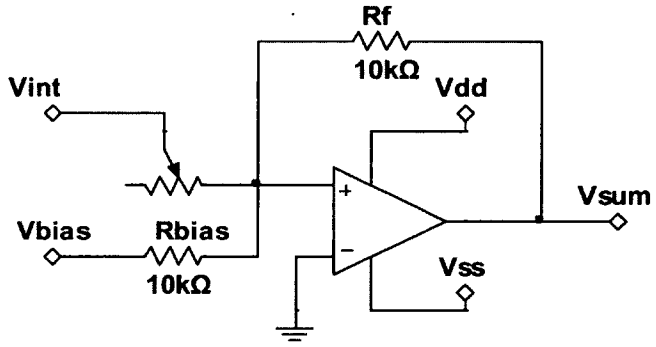


Figure 2.15: Summing Amplifier Circuit Schematic

$$V_{SUM} = -\left(V_{INT}\left(\frac{R_F}{R_{POT}}\right) + V_{BIAS}\left(\frac{R_F}{R_{BIAS}}\right)\right) \quad (2.3)$$

which simplifies to:

$$V_{SUM} = -\left(V_{INT}\left(\frac{R_F}{R_{BIAS}}\right) + V_{BIAS}\right) \quad (2.4)$$

2.5.5 Output Filter

The final stage is a low pass filter responsible for filtering the output to prevent high frequency oscillations and noise on the VCO input. The filter is in an inverting configuration because the summing amplifier is also inverting, and its output cannot be sent straight to the VCO tuning pin. The output filter is a first order filter with the cutoff frequency:

$$f_c = \frac{1}{2\pi RC} \tag{2.5}$$

For the values in Figure 2.16, the cutoff frequency is $f_c \cong 995\ Hz$, yielding a system bandwidth of approximately 1 kHz.

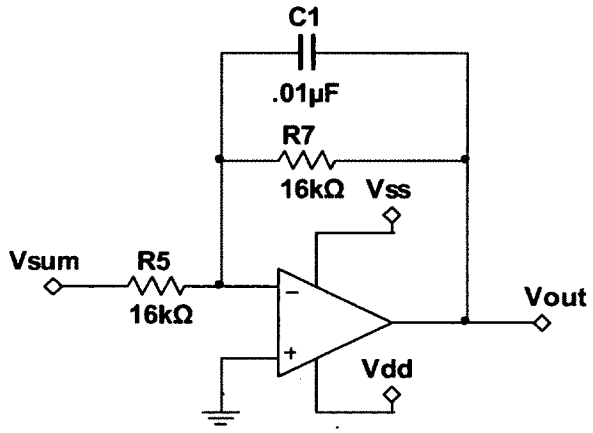


Figure 2.16: Output Filter Circuit Schematic

2.5.6 Control Circuit Output

The control circuit uses the RF circuit to measure the response of the IDC sensor as a function of frequency with the magnitude/phase detector. The control circuit adjusts the tuning voltage to the VCO appropriately to maintain a constant voltage out of the magnitude/phase detector. The final equation for the circuit:

$$V_{TUNE} = \left(V_{BIAS} * \left(\frac{R_F}{R_{BIAS}}\right)\right) + \left(\frac{1}{R_{int}C_1}\int (V_{MEAS} - V_{HOLD}) * \left(\frac{R_F}{R_{POT}}\right) dt\right) \tag{2.6}$$

The final equation in a simplified form:

$$V_{TUNE} = V_{BIAS} + K\int (V_{HOLD} - V_{MEAS})dt \tag{2.7}$$

where the gain of V_{BIAS} is unity, and K is a gain factor encompassing both the time constant of the integrator and gain for summing amplifier. The full schematic can be found in Appendix D.

2.6 Tracking Circuit Simulation

The circuit was simulated in National Instruments Multisim. A basic op-amp model was used for each stage to test for functionality. The testing consisted of applying known inputs to the system, and probing the circuit after each stage to confirm the behavior matches the theory as described by Equation (2.7). A square wave at 100 Hz added in series with the input for V_{MEAS} causes the integrator output to respond, ultimately increasing the final output according to theory. Figure 2.17 shows the response of the entire tracking circuit to a 100 Hz square wave. The dashed line in Figure 2.17 represents the input the integrator, and the response confirms that for a non-zero difference at the input of the circuit, the output will adjust appropriately, in this case increasing until the difference at the input returns to zero. The schematic can be found in Appendix D.

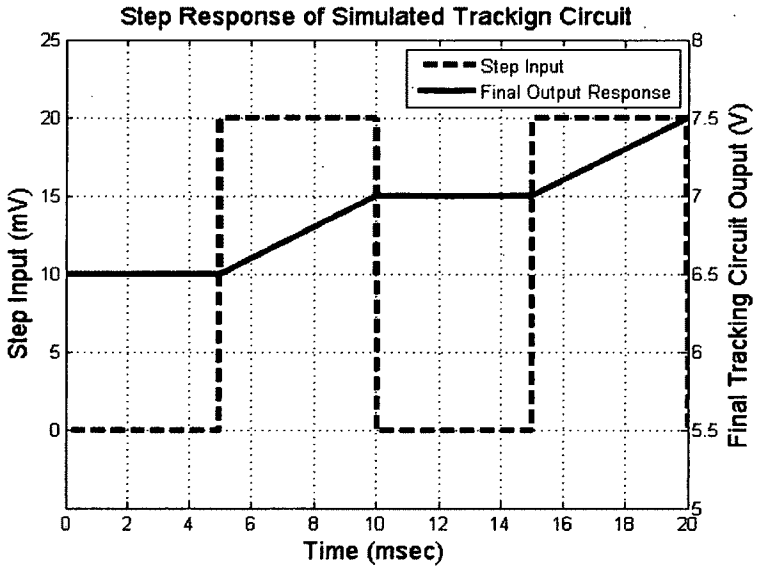


Figure 2.17: Step Response of Simulated Circuit

2.7 Data Acquisition Device

The first and last element in the signal chain for this circuit is the external data acquisition device, the National Instruments NI-6211 USB DAQ, pictured in Figure 2.18.

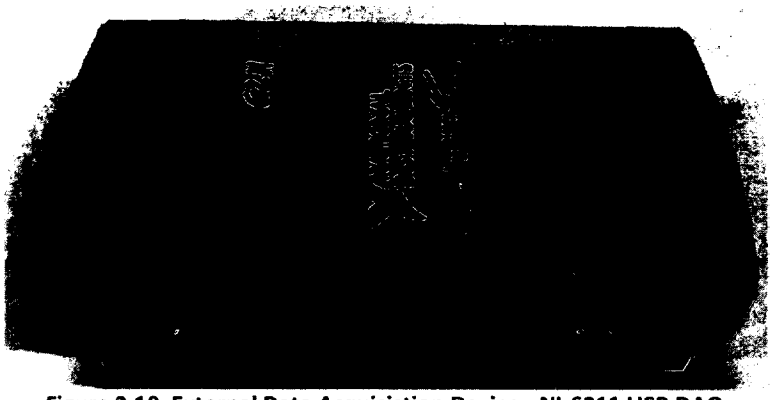


Figure 2.18: External Data Acquisistion Device - NI-6211 USB DAQ

This device connects to the computer via USB, and has terminal blocks to connect to the system. The device is controlled by National Instruments LabVIEW software. The device has two digital-to-analog converters (DAC) and eight differential analog-to-digital converters (ADC). The NI-6211 generates the analog voltage to tune the VCO, and reads the output of the magnitude/phase detector analog voltage channels. The DAC and ADC are both 16-bit resolution converters. Detailed specifications of the device are shown in Appendix B.

2.8 Fabrication

The circuit was fabricated in the lab using the LPKF S62 PCB Prototyping Machine. The properties of the material used for fabrication are shown in Table 2.2 [10].

Table 2.2: Prototyping Material Properties

Property	Value
Insulator Material	FR4
Insulator Thickness (mil / μm)	28 / 711
Insulator Relative Permittivity (ϵ_r)	4.34
Copper Weight (oz.) / Copper Thickness (μm)	0.5 / 17.5

The PCB traces for the RF signals require special attention because the RF signals need a transmission line with a constant impedance, in this case 50Ω. If the impedance of the transmission line formed by the PCB trace is not properly matched to the devices along the transmission line that are designed for a 50Ω system, such as the VCO, the reflections at the

boundary between two different impedances will negatively affect circuit performance. The traces were designed as microstrips for the two-layer design in this thesis, where a ground plane must exist under the RF traces, as seen in Figure 2.19, which labels the dimensions for the trace width, W, trace thickness, T, and height from the ground plane, H. The differences in copper thickness between the top and bottom layers is part of the illustration. The fabricated circuit has the same amount of copper per unit area on both sides.

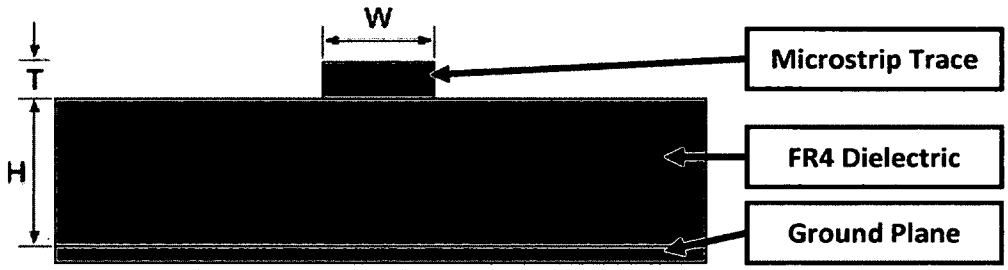


Figure 2.19: Microstrip PCB Trace

The dimensions of the microstrip determine its impedance. The expression that has been proven to provide reliable estimates of the trace impedance with limited computational complexity is the empirical expression [11]:

$$Z_0 = \frac{Z_f}{\sqrt{\epsilon_{eff}} * \left(1.393 + \frac{w}{h} + \frac{2}{3}\ln\left(\frac{w}{h} + 1.444\right)\right)} \quad (2.8)$$

with

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} * \left(1 + 12\left(\frac{h}{w}\right)\right)^{-\frac{1}{2}} \quad (2.9)$$

and

$$Z_f = \sqrt{\frac{\mu_0}{E_0}} = 376.8\Omega \quad (2.10)$$

where Z_f is the free space impedance, ϵ_r is the relative permittivity of the dielectric material, ϵ_{eff} is the effective dielectric constant, and w and h are the width of the trace and height from the ground plane, as shown in Figure 2.19.

The empirical expression to solve for the trace width required for a desired transmission line impedance is [11]:

$$w = \frac{8e^A}{e^{2A} - 2} * h \tag{2.11}$$

with

$$A = 2\pi * \frac{Z_0}{Z_f} * \sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1} * \left(0.23 + \left(\frac{0.11}{\epsilon_r}\right)\right) \tag{2.12}$$

Implementing the expressions above for a material thickness, h, of 0.028 inches and ϵ_r of 4.34, to solve for the trace width for an impedance of 50Ω resulted in a value of 0.052 inches. Solving for the impedance with Equation (2.8) based on the trace with 0.052 inches results in an impedance of 50.2Ω, which is within 0.5% of 50Ω. Each trace that transmits an RF signal has a trace width of 0.052 inches, and the entire RF section of the board has a ground plane below it.

Surface mount components are used wherever possible for multiple reasons. Surface mount components are physically smaller than through-hole components, and are available in several sizes for different applications and design requirements. Most passive components, such as resistors and capacitors, for this design are the Imperial size code 0603, meaning they are 0.063 inches long by 0.031 inches wide. The small size lends itself to a more compact and simpler PCB trace layout. The fact that surface mount components do not need holes drilled for the leads simplifies layout design and fabrication. Another reason for their use is that the low noise amplifiers required in the design are only available in surface mount packages, and using

surface mount passive components significantly reduces layout complexity and layer-to-layer via count. Figure 2.20 shows the difference in size between an Imperial size 0603 surface mount resistor and a ¼ W through-hole resistor.

Figure 2.20: Surface Mount Resistor (bottom) vs. Through-Hole Resistor (top)

The circuit board needs two connections, one to communicate with the external data acquisition device, and another to supply power. Both connectors are shielded, and use shielded cables with ferrite beads on each end of the cable to suppress radiation to and from the device. The data is transferred over an Ethernet cable, and uses a standard RJ-45 connector. The Ethernet cable has four sets of twisted pairs, allowing four differential signals to transfer in either direction. It should be noted that the circuit does not use the Ethernet protocol or any other data communication standard.

The power is supplied by means of an eSATA connection, chosen for two reasons. It has sufficient outputs to supply a positive and negative supply voltage, and is not interchangeable with the Ethernet connector for data, thus preventing potential damage to the circuit from a connection error. The physical connections are shown in Figure 2.21.

Figure 2.21: Power Connector on the left, and Data Connector on the right

A custom PCB breakout adapter was fabricated to allow the Ethernet cable to connect to the data acquisition device without cutting the end of the Ethernet cable and individually connecting each signal line to the terminal blocks of the device. The adapter decreases experimental setup time, and increases modularity by allowing any Ethernet cable to be used without stripping one end. Another advantage of the adapter is the switch used for signal routing depending on the application. The total number of data lines required for both the diagnostic and tracking mode is greater than the number of data lines available on the Ethernet cable. The switch on the breakout adapter allows one of the data lines of the Ethernet cable to be used for either an ADC input in diagnostic mode, or DAC output in tracking mode. The custom breakout adapter is pictured in Figure 2.22.

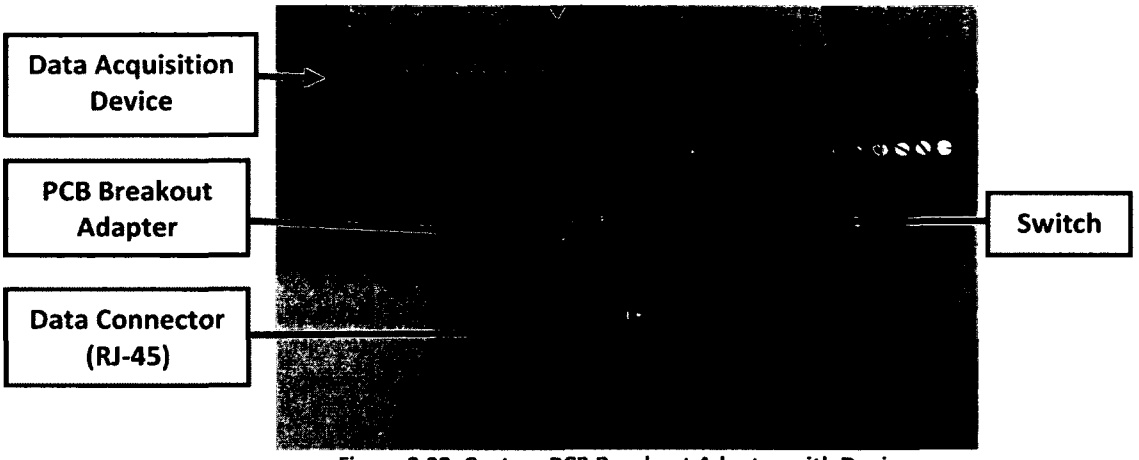


Figure 2.22: Custom PCB Breakout Adapter with Device

The entire fabricated circuit is pictured in Figure 2.23, with the RF components and analog components each highlighted. The RF components are housed inside an RF shield, discussed further in Chapter 3.

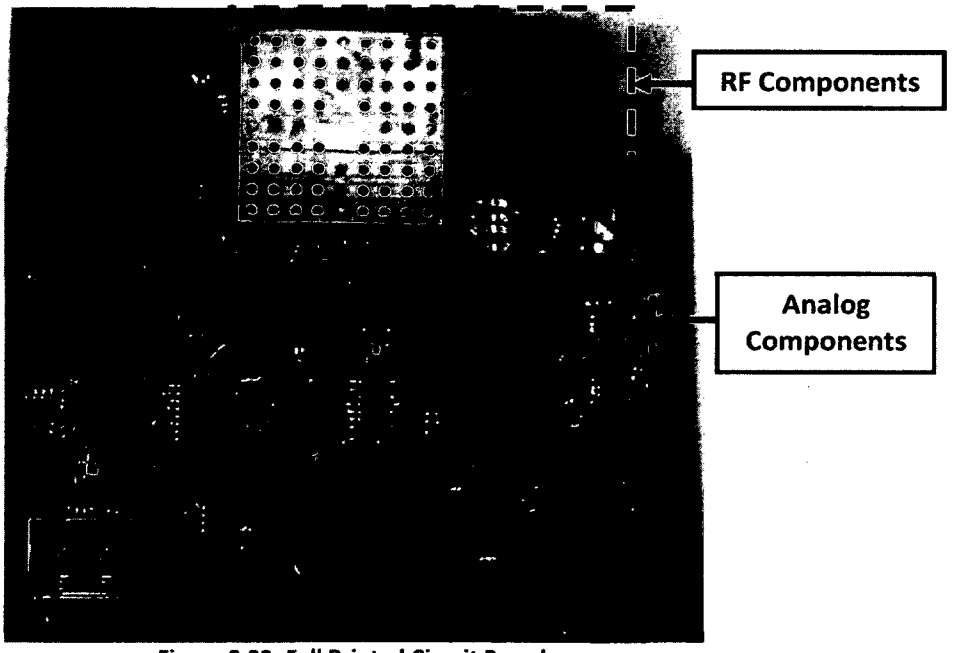


Figure 2.23: Full Printed Circuit Board

2.9 Summary

The circuit is designed to measure the resonant frequency of the IDC sensor, and track the changes in response to strain. The circuit is initially operated in the open-loop diagnostic mode

to identify the resonant frequency of the IDC sensor. The analog output from the external DAC provides a tuning voltage to the VCO, in turn generating an RF signal. This RF signal propagates through both a controlled reference trace, and the probe loop trace that couples with the IDC sensor. The frequency response of the IDC sensor couples onto the probe loop, and the magnitude/phase detector compares the test and reference RF signals. The difference in magnitude and phase between the reference and test signals is represented as an analog voltage on two separate output channels.

The closed-loop analog tracking circuit design facilitates the measurement of the strain on the tool by measuring the change in resonant frequency. The tracking circuit responds to changes in the resonant frequency and adjusts the VCO input voltage to maintain a constant value out of the magnitude/phase detector. The circuit was simulated using NI Multism, and the design proved to successfully adjust the final output due to a known change at the input. The analog tracking circuit is critical to measuring the strain on the tool without contacting the tool.

The design was fabricated in the lab on a two-layer PCB. The RF traces require a specific, calculated trace width of 0.052 inches, with a constant ground plane below to properly propagate the RF energy. Surface mount components allow the design to be more compact with a simpler layout than through-hole components. The circuit layout is just as important as the design to ensure proper functionality.

CHAPTER 3

Noise in Electronic Circuits

3.1 Introduction

Noise is the undesired random fluctuation that obscures or otherwise interferes with the signal of interest and is present in any electronic device [12]. Not all noise is equal however, as there are multiple different ways for noise to couple to a signal. This chapter provides an overview of noise in an electronic system and different techniques to minimize the effect of noise. Appendix C discusses noise measurement and calculation in detail, and provides a statistical overview of how the standard deviation relates to noise measurement and calculation.

3.2 Types of Noise

Two basic types of noise affect electronic circuits, white noise and pink noise. Each draws their name from the color of the light in the visible spectrum with similar properties.

White noise is a random signal with a flat power spectral density. The thermal noise of a resistor, Johnson noise, and the majority of the noise spectrum of an operational amplifier, is white noise in nature. Figure 3.1 shows the spectral density plot of zero mean white noise simulated in Matlab [13].

Pink noise is also a random signal, but the power spectral density decreases by 3 dB/octave. Therefore, the power in the noise signal decreases linearly with an increase in frequency, giving

rise to its alternative name, $1/f$ noise. The cutoff where the noise shifts from pink to white is the 1/f corner frequency, with a lower corner frequency preferable for most applications. Figure 3.2 shows the simulated spectrum of pink noise for a device with a 1/f corner frequency of 100 Hz.

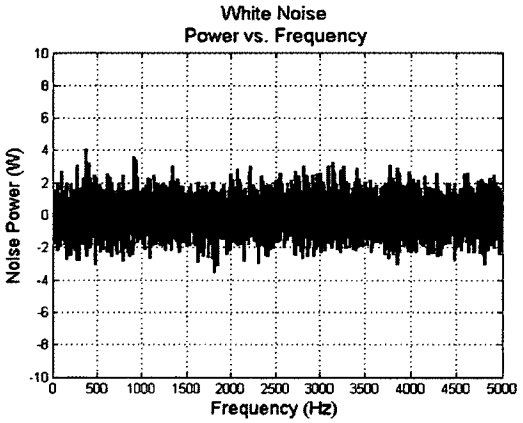


Figure 3.1: Spectrum of White Noise

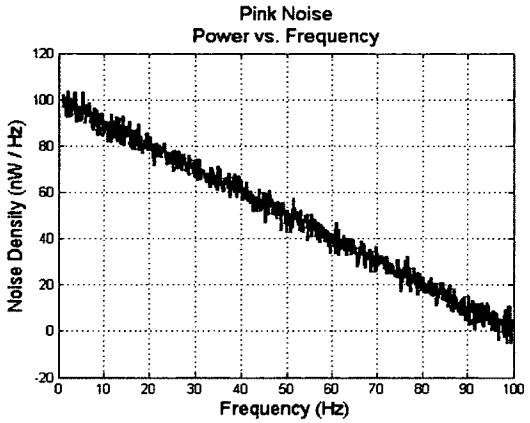


Figure 3.2: Spectrum of Pink Noise

Noise is a factor in every active and passive component of an electronic circuit. The noise power produced from a conductive device is a function of the temperature of the device and the bandwidth of the system [12]:

$$N = kTf_{bw} \tag{3.1}$$

where N is the noise power,

$k = 1.38 * 10^{-23} Joules/degree\ Kelvin$ (Boltzmann's Constant), $T =$ Temperature in Kelvin, and f_{bw} is the system bandwidth. Equation (3.1) shows that the noise, N, is white noise because the total noise power will increase linearly with the system bandwidth.

3.3 Resistor Noise

The noise power generated by a resistor, also known as Johnson noise, is very similar to the general conductor noise equation in Equation (3.1):

$$N_R = 4kRTf_{bw}\ (V_{RMS}^2) \tag{3.2}$$

where R is resistance. From Equation (3.2), it can be seen that the noise in a resistor is also white noise in nature, because the noise power, N_R,increases linearly with bandwidth. To define the noise is terms of voltage, Equation (3.3)shows the root-mean-square voltage noise is found by taking the square root of N_R:

$$V_{nR} = \sqrt{N_R} = \sqrt{4kRTf_{bw}}\ (V_{RMS}) \tag{3.3}$$

which simplifies at room temperature to:

$$V_{nR} = 0.128 * \sqrt{Rf_{bw}}\ (nV_{RMS}) \tag{3.4}$$

It can also be useful to put resistor noise in terms of $nV/\sqrt{Hz}$ to provide a single value as a function of the square root of the bandwidth:

$$V_{nRf} = \sqrt{4kRT}\ (nV/\sqrt{Hz}) \tag{3.5}$$

The noise power and V_{RMS} noise of a 1 $k\Omega$ resistor at room temperature as a function of the frequency bandwidth is shown in Figure 3.3, where the noise power is on the order of $10^{-12}\ Watts$, and the V_{RMS} noise is on the order of $10^{-6}\ V_{RMS}$. These values are orders of magnitude smaller than the measured noise levels of the circuit in this thesis, but understanding the impact of a resistor is important in low noise design and component selection, as demonstrated in this chapter as well as Appendix C.

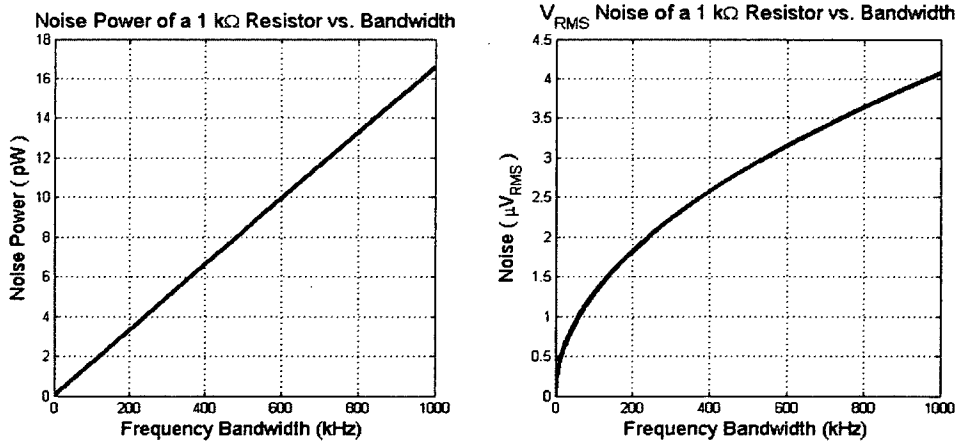


Figure 3.3: RMS Noise of Resistor vs. Bandwidth

3.4 Operational Amplifier Noise

Noise from an active component such as an Operational Amplifier (op-amp) is more complicated than passive components, and this section will focus on the noise generated within op-amps, not the effect of external noise coupling into the device. Op-amps suffer from both white noise and pink noise. The white noise makes up the majority of the device's bandwidth, while the pink noise dominates at low frequencies. A typical spectrum for an op-amp noise density is plotted in Figure 3.4.

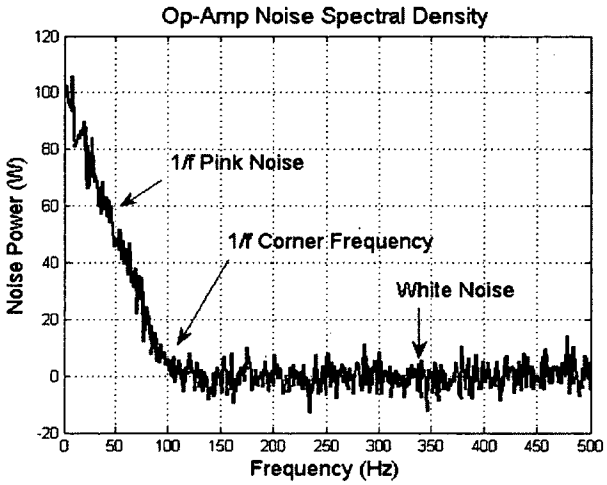


Figure 3.4: Typical Op-Amp Noise Spectral Density

There are three main factors to consider when calculating op-amp circuit noise; the voltage noise and current noise of the device, as well as the Johnson noise of a resistor. The voltage noise and current noise are listed by the manufacturer as a function of the bandwidth in terms of $nV/\sqrt{Hz}$ and $pA/\sqrt{Hz}$ or $fA/\sqrt{Hz}$, respectively. Specified voltage and current noise values are associated with an integrated circuit design, but not to each individual part [13].

The voltage noise of an op-amp is a function of the device itself and is the result of the random fluctuation internally within the op-amp. The voltage noise is modeled as a voltage source in series with the input terminal of a noiseless op-amp, shown in Figure 3.5. Typical values for voltage noise are between $1\ nV/\sqrt{Hz}$ and $20\ nV/\sqrt{Hz}$.

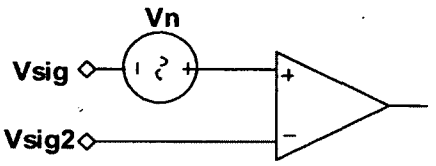


Figure 3.5: Voltage Noise Model for an Op-Amp

An ideal op-amp has no current flowing into the device, but there is always a small non-zero bias current into each terminal of a real op-amp. Current noise is the fluctuation of the current that flows into both input terminals, and is only a factor when it is flowing through an external resistor, thus creating a voltage noise. The current noise varies across devices much more than the voltage noise, and can range from $0.1fA/\sqrt{Hz}$ to $20\,pA/\sqrt{Hz}$. Current noise is specified as a single value, but is present on both input terminals. The current noise is modeled as a voltage source representative of the voltage drop across an input resistor, and Figure 3.6 shows both a current source leading into a resistor, and the simplified voltage source model.

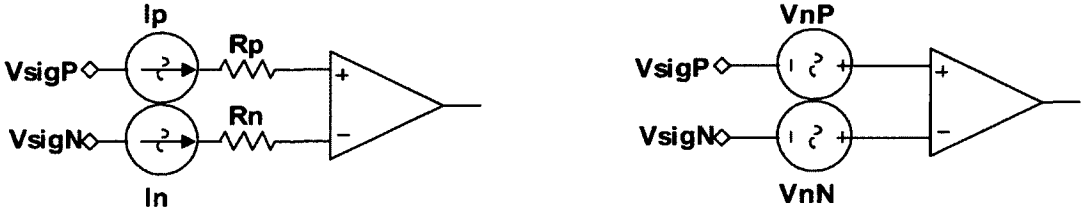


Figure 3.6: Current Noise Model for an Op-Amp

The bandwidth of the system must be known in order to properly calculate the total noise power. When the bandwidth is orders of magnitude greater than the 1/f corner frequency, the broadband white noise will dominate the total noise, and the 1/f noise can be ignored. If the system bandwidth is closer to the 1/f corner frequency then the impact of the pink noise must be considered. The noise contribution below the 1/f corner frequency is the integral of the function that represents the pink noise, bounded by the bandwidth. For the V_{RMS} noise at or below the 1/f corner frequency in the bandwidth of f_l to f_c [14]:

$$V_{np} = V_n * \sqrt{f_c} * \sqrt{\int_{f_l}^{f_c} \frac{1}{f} df} = V_n * \sqrt{f_c * \ln\left(\frac{f_c}{f_l}\right)} \ (V_{RMS}) \quad (3.6)$$

where V_{np} is the resultant V_{RMS} noise in the 1/f region, f_c is the 1/f corner frequency, f_l is the lower frequency bandwidth cutoff, and V_n is the white noise of the device.

To calculate the expected noise contribution for a device with a known system bandwidth, begin with the specified voltage noise spectral density and current noise spectral density from the device datasheet. The measurement of the noise spectral density for an op-amp is detailed in Appendix C. The ADA4004-4 op-amp from Analog Devices noise density is shown in Table 3.1. The voltage noise for less than 10 Hz is specified as a peak-to-peak voltage because the bandwidth is already defined, whereas the noise density is provided for applications where white noise will dominate. This definition allows the designer to calculate the total noise depending on the bandwidth of the system implemented. Figure 3.7 and Figure 3.8 show the plot for the voltage noise density and current noise density of the device respectively [15]. The 1/f corner frequency for the voltage noise density is approximately 10 Hz, while the corner frequency for the current noise is approximately 100 Hz.

Table 3.1: Manufacturer Specified Noise Performance for ADA4004-4 Op-Amp

Measurement	Bandwidth	Value
Voltage Noise	0.1 Hz to 10 Hz	$0.15(\mu V_{pp})$
Voltage Noise Density	1 kHz	$1.8\ nV/\sqrt{Hz}$
Current Noise Density	200 Hz	$1.2\ fA/\sqrt{Hz}$

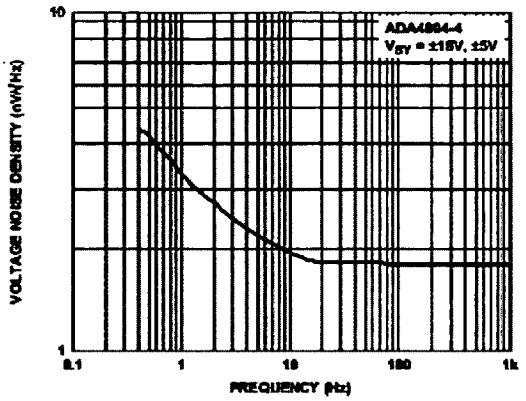


Figure 3.7: Voltage Noise Density vs. Frequency

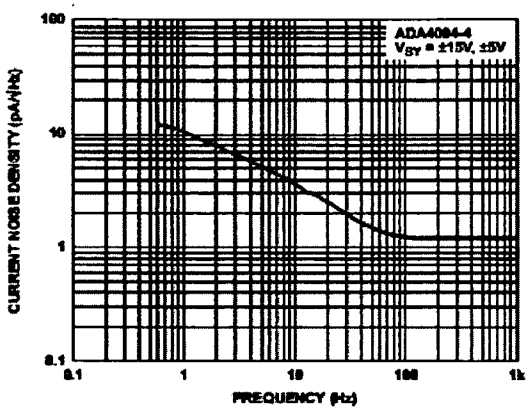


Figure 3.8: Current Noise Density vs. Frequency

The voltage noise of the device for a particular bandwidth beyond the 1/f corner frequency is:

$$V_{nSys} = V_n * \sqrt{f_{bw}}\ (nV_{RMS}) \tag{3.7}$$

The square root of the bandwidth is required because the unit of noise density is $nV/\sqrt{Hz}$, so multiplying by $\sqrt{Hz}$ will result in nV_{RMS}. The result, V_{nSys}, is an RMS voltage, which is equivalent to one standard deviation if the mean is zero, which is true for white noise. The statistics of noise and quantifying peak-to-peak noise is discussed in Appendix C, and approximated by six standard deviations, $\pm 3\sigma$, to represent 99.7% of the data:

$$V_{nPP} = 6 * V_{nSys}\ (nV) \tag{3.8}$$

For a system with a $10\ kHz$ bandwidth, the peak-to-peak voltage noise contribution for the ADA4004-4 is:

$$6 * \left(\frac{1.8\ nV}{\sqrt{Hz}} * \sqrt{10\ kHz}\right) = 1.8\ \mu V_{pp} \tag{3.9}$$

The peak-to-peak noise value from Equation (3.9) is the voltage noise contribution of a single device to the total noise, and is much smaller than the measured values for total system noise that are seen in Chapter 4.

Calculating the total noise of the system including the current noise and Johnson noise is demonstrated in more detail in Appendix C.

3.5 Frequency Spectrum Noise

When working with oscillators and other devices that operate at fixed frequencies, the noise is often calculated in the frequency domain as opposed to the time domain. This section uses several figures to aid in illustrating the concepts of noise in the frequency domain, where the figures are based on a modeled 2 kHz sine wave sampled at 20 kHz to avoid the computational load of modeling frequencies of approximately 1 GHz. The concepts explained here apply equally to higher frequency signals where the VCO and IDC sensor operate. The effect of oscillator noise is presented in both the time domain and frequency for additional clarity. The equation for a wave at a particular frequency in the time domain is:

$$y(t) = Acos(2\pi ft + \phi) \tag{3.10}$$

where $y(t)$ is the resultant signal at a particular time step, A is the amplitude of the oscillation, f is the frequency, t is the current time step, and ϕ is the offset phase angle. For an ideal sine or cosine wave, the quantity representing the instantaneous phase angle, $(2\pi ft + \phi)$, increments around the unit circle from 0 to 2π at a rate defined by the frequency, f. Figure 3.9 shows an example of the angle propagating around the unit circle with amplitude A, at a point in time where the angle is $\pi/4$. A higher frequency will propagate around the unit circle faster, completing more full cycles in the same time as a lower frequency.

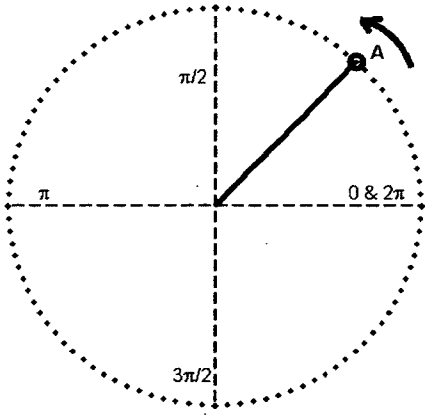


Figure 3.9: Angle of a Wave Propagating Around the Unit Circle with Amplitude A

The plot of the phase angle vs. time sample and the resultant sine wave without any added noise are both shown in Figure 3.10, and the frequency domain plot is shown by the FFT in Figure 3.11.

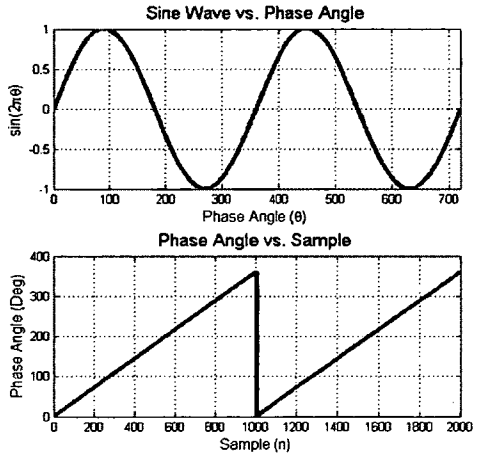


Figure 3.10: Phase Linearly Inreasing to form Sine Wave

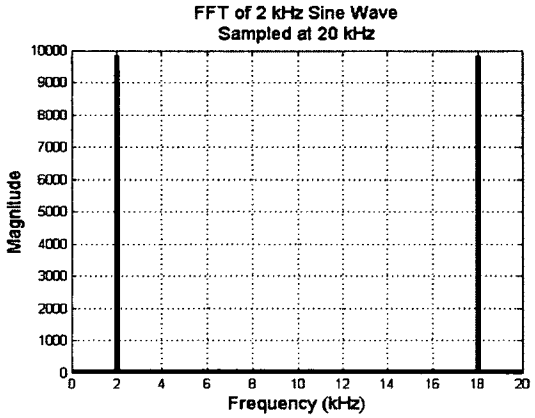


Figure 3.11: FFT of 2 kHz Sine Wave

Any noise in the phase angle as it propagates around the unit circle will result in a noisy instantaneous frequency. Therefore, the figure of merit for noise in oscillators and frequency generators is phase noise. The phase noise of an oscillator can be expressed as [16]:

$$L(f_m) = 10\log_{10}\left(\frac{FkT}{2P_s} * \left(1 + \frac{f_c}{f_m} + \left(\frac{f_0}{2f_m Q_L}\right)^2 * \left(1 + \frac{f_c}{f_m}\right)\right)\right) dBc/Hz \quad (3.11)$$

where F is the noise factor, defined as the ratio of the signal-to-noise ratio of the input to the signal-to-noise ratio of the output [16]:

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} \quad (3.12)$$

and k is Boltzmann's Constant, T is temperature in Kelvin, P_s is the output power of the oscillator, f_0 is the output frequency, f_m is the offset from the output frequency, f_c is the 1/f cutoff frequency, and Q_L is the loaded Q factor of the oscillator. The phase noise is defined in terms of dBc/Hz, where dBc is decibels with respect to a carrier, in this case the desired output

frequency, and is a function of the offset from the desired output frequency in terms of Hz. The phase noise of a VCO is specified at multiple values of f_m, often including 1 kHz, 10 kHz and 100 kHz. Figure 3.12 compares an ideal sine wave to an ideal sine wave with simulated phase noise added. The simulated phase noise shown is large enough to demonstrate the effect in the time domain. Note that the peaks of the ideal sine wave and noisy sine wave do not always correspond to each other, resulting in instantaneous frequency variations.

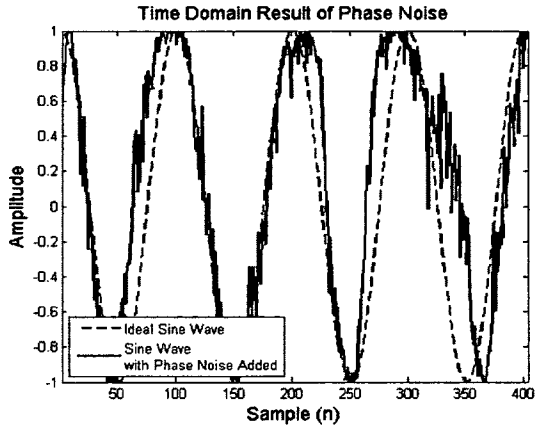


Figure 3.12: Time Domain Plot of Ideal Sine Wave and Sine Wave with Phase Noise

The frequency domain result of adding phase noise to a 2 kHz sine wave is shown in Figure 3.13. The plot demonstrates the effect of phase noise in the frequency domain, with a lower amplitude and wider peak at the carrier frequency because more energy is spread across the spectrum.

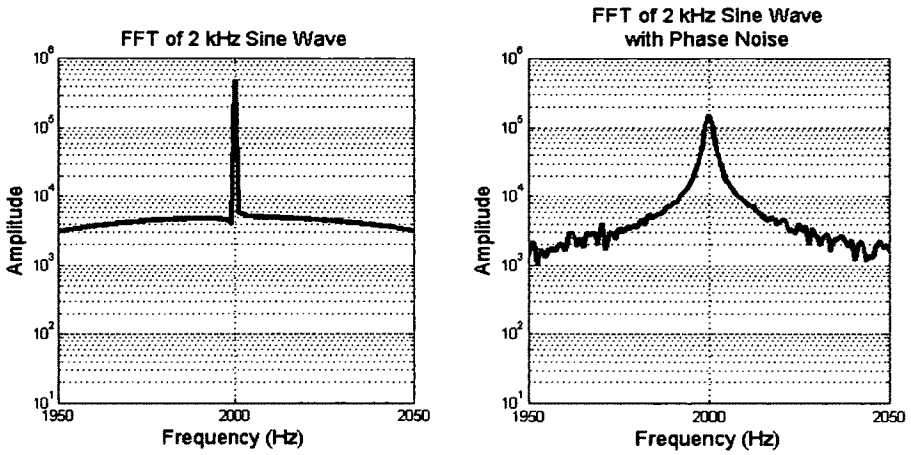


Figure 3.13: Comparison of Ideal Sine Wave FFT and Sine Wave with Phase Noise FFT

Spurious frequency spikes, also known more simply as spurs, are also a concern when working with oscillators. Spurious frequencies are content above the noise floor that is outside the desired frequency output of the oscillator. The spurious content can be harmonically related, but are not explicitly a harmonic of the carrier frequency. Spurious frequency spikes are measured in dBc similar to phase noise. Figure 3.14 shows a frequency domain plot of a 2 kHz sine wave with the same amount of phase noise as seen in Figure 3.13, but also features spurious frequency spikes.

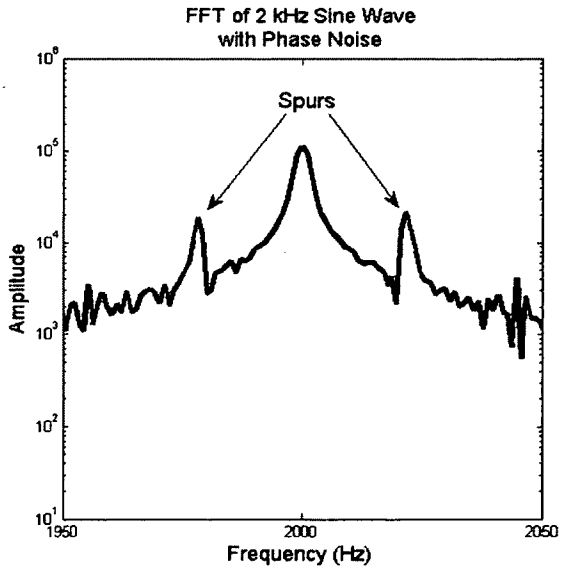


Figure 3.14: FFT of Sine Wave with Phase Noise and Frequency Spurs

Understanding the effect of phase noise on the output of an oscillator and the manufacturer's specified levels of phase noise is very important in this application. The phase noise of the oscillator must be low enough as to not dominate the response of the IDC.

3.6 Printed Circuit Board Noise Considerations

The design of a printed circuit board (PCB) can also have an impact on the noise of the circuit. The designs created for this thesis are two-layer circuit boards, manufactured in the lab. When laying out a two-layer circuit board for low noise, the power supply network, component placement and signal routing are critical.

The power and data connections for the circuit are both made with a shielded cable and terminated by the proper jack at both ends, with the jack tied to ground. Each cable also features a ferrite bead at each end to help noise suppression. The shielded cables help reduce unwanted noise coupling onto the signals between the PCB and the data acquisition device.

To reduce the effect of electromagnetic radiation from the VCO coupling into the probe loop or IDC sensor loop, a PCB mounted RF shield was placed over the RF components. Figure 3.15 shows the base of the shield with the components inside, and Figure 3.16 shows the RF shield with the top cover in place.

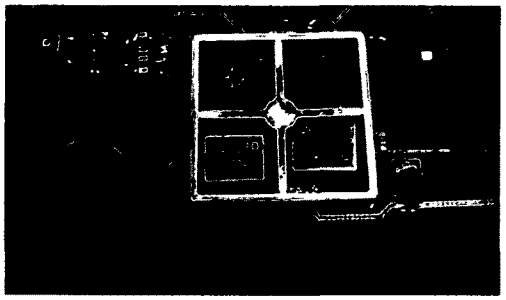


Figure 3.15: RF Components Inside Shield

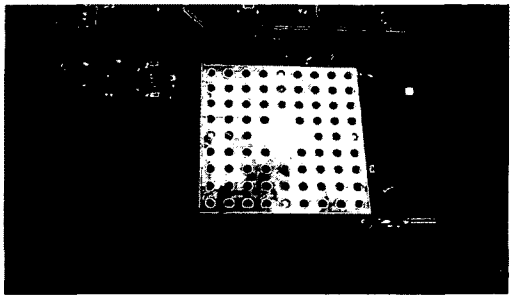


Figure 3.16: RF Shield with Top Cover

The power supply network includes the traces that provide power to each active device on the board. The power supply traces themselves should be wide to present as low impedance as

possible [17]. The power supply traces for the design in this thesis were 0.040 inches wide. Every device has high-frequency bypass capacitors between the power supply trace and ground, positioned as close to the device as possible. When multiple capacitors are used as a shunt to ground for high-frequency noise, the smallest value capacitor is the closest to the device, ensuring that the highest frequency noise content is shorted to ground just before the signal enters the device. To facilitate the use of bypass shunt capacitors to ground, the ground plane extends across the entire board with analog signals routed on the ground layer only when routing on the top layer is too long and convoluted or impossible. Figure 3.17 shows two capacitors used to suppress noise on the power supply trace of an IC, where each capacitor has its own via to the ground plane. Based on information from B. Carter [18], the high frequency bypass capacitors were selected to be $10\mu F$ and $0.1\mu F$.

Figure 3.17: Power Supply Noise Suppression Shunt Capacitors

Signals require a return path in order for current to flow. The ground plane makes this much simpler, but some signals may need to be routed on the bottom layer. If a signal trace exists on the bottom layer in the path of a return current, the current will be forced to take a longer path. Adding a break in the ground plane can be used to force return currents away from sensitive components. Figure 3.18 illustrates the possible paths for return currents with a gap in

the ground plane to protect sensitive components [19]. The PCB layout including both the top and bottom layer can be found in Appendix D.

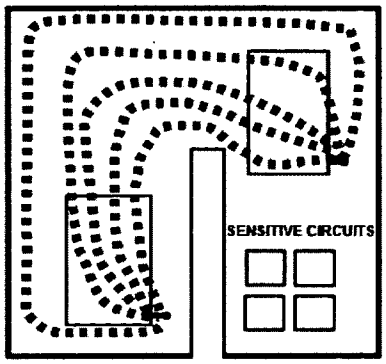


Figure 3.18: Return Currents on PCB with Ground Plane Gap

3.7 Circuit Component Noise Performance

The most important factor affecting the achievable resolution for this application is the amount of noise present in the system. The total noise is primarily a function of variations in the output frequency from the VCO, the noise introduced by the magnitude/phase detector, and the noise caused by the amplifiers. This section discusses the noise levels of the RF components and the analog amplifiers for the tracking circuit.

3.7.1 Voltage Controlled Oscillator

Noise on the tuning voltage applied to the input to the VCO is the main contributor to output frequency noise, with frequency pushing, phase noise, and spurious frequencies also factors to consider. If the VCO is treated as an ideal transfer function, the noise on the tuning voltage will affect the output frequency according to the transfer function in Figure 2.3. The slope of the VCO sensitivity with respect to the input voltage is shown in Table 3.2.

Table 3.2: ROS-2230-119+ Sensitivity

Voltage Input (V)	Frequency Output (MHz)	Sensitivity (MHz/V)
0.5	1131.3	124
1	1193.4	127
2	1318.2	116
3	1425.2	100
4	1521.3	91
5	1610.3	74
6	1685.9	78
7	1759.2	63
8	1816.8	68
9	1898.3	65
10	1968.1	80

A higher sensitivity for the VCO will result in a higher frequency shift for a given voltage shift. The resonance peak from Figure 2.4 is at approximately 1400 MHz, where the VCO has a sensitivity of over 100 MHz/V. This means, for a frequency noise value less than 10 kHz, the voltage noise must be less than $100\ \mu V$.

The phase noise, spurious frequency, and frequency pushing performance are shown in Table 3.3. Figure 3.19 shows a plot of the phase noise for the ROS-2230 VCO from the manufacturer specifications[9]. The discrete points of the phase noise plot are points are from the information in Table 3.3.

Table 3.3: VCO ROS-2230 Output Frequency Performance

Phase Noise (dBc/Hz) (at offset frequencies)	**1 kHz**	-70
	10 kHz	-99
	100 kHz	-120
	1 MHz	-141
Non Harmonic Spurious (dBc)	-90	
Frequency Pushing (MHz/V)	0.7	

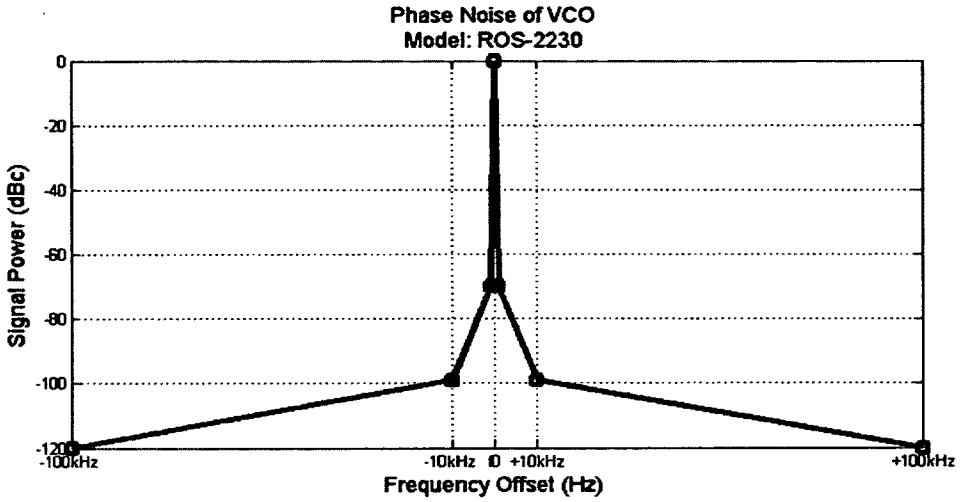


Figure 3.19: Phase Noise of ROS-2230 VCO vs. Offset Frequency

From Table 3.3, the phase noise and non-harmonic spurious frequencies are never greater than 70b dB below the desired output frequency. Figure 3.20 compares a plot of the magnitude response of the IDC sensor in dB and the specified VCO phase noise in dB. The VCO phase noise appears as a single line because the bandwidth is so narrow compared to the width of the sensor response. Since the phase noise has a much smaller bandwidth that the IDC sensor response, the phase noise was not included in the model discussed in Section 3.8.

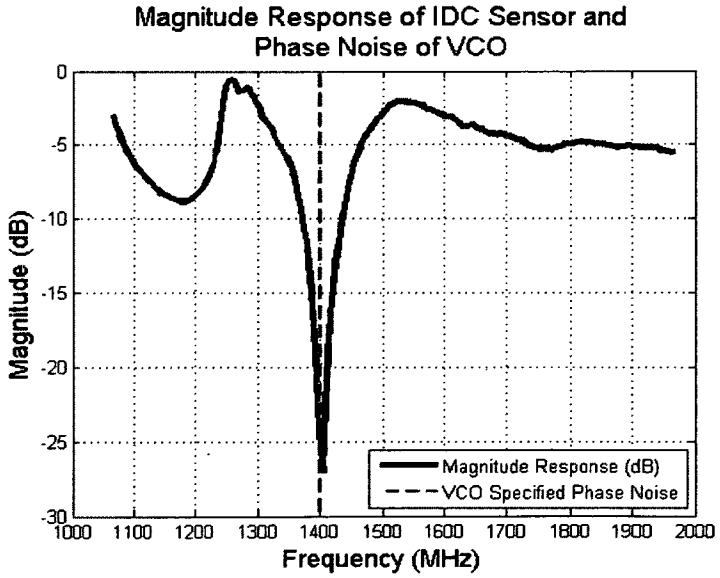


Figure 3.20: Magnitude Response of IDC Sensor and VCO Phase Noise

To minimize frequency pushing, the shift in the VCO output frequency caused by fluctuations in the power supply, the VCO was powered by a 12 V Low Dropout Linear Regulator (LDO), the LM78L12, which has a specified output voltage noise of 40 μV. From the frequency pushing metric in Table B.1, the calculated corresponding output frequency shift is:

$$40\ \mu V * \frac{700\ kHz}{V} = 28\ Hz \tag{3.13}$$

which is negligible compared to the output frequency of the VCO, over 1 GHz. The dominant factor for the noise of the VCO is therefore the noise on the tuning voltage input of the device.

3.7.2 Magnitude/Phase Detector

The magnitude/phase detector has its own characteristics that must be considered to properly understand the performance of the RF circuit. The output noise of the magnitude/phase detector is specified in terms of voltage noise spectral density, similar to the discussion in Section 3.4 for operational amplifiers. The plots from the datasheet in Figure 3.21 and Figure 3.22 represent the density of noise in units of $nV/\sqrt{Hz}$ [8]. Since the specified noise is in terms of the system bandwidth, to get a more meaningful value in terms of V_{RMS} or V_{PP}, the bandwidth of the system must be known in order to compare the specified noise with the V_{RMS} or V_{PP} that was measured. Each output of the magnitude/phase detector has an output filter pin for use with an external filter capacitor to ground, C_{FLT}, to adjust the bandwidth, as determined by:

$$f_{bw} = \frac{1}{2\pi * 3300 * (C_{FLT} + 1.5pF)} \tag{3.14}$$

If no filter capacitor is used, the output bandwidth is just over 32 MHz, which corresponds to the maximum value of the frequency axis in Figure 3.21 and Figure 3.22.

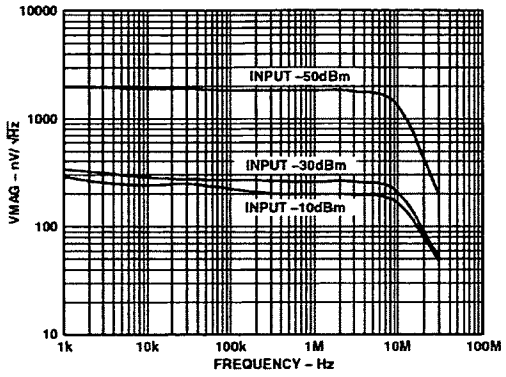


Figure 3.21: Magnitude Output Noise Spectral Density vs Frequency

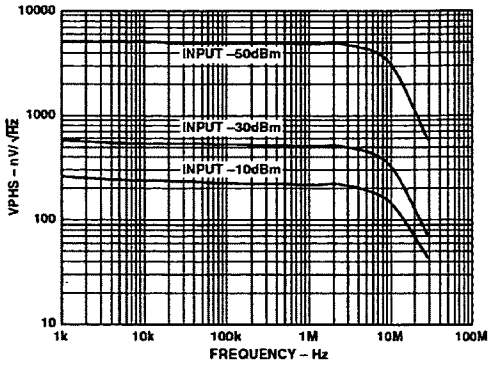


Figure 3.22: Phase Output Noise Spectral Density vs. Frequency

The value of the noise density taken from Figure 3.21 and Figure 3.22 depends on the power level of the input RF signal. Since the input power is approximately -4dBm, the -10dBm trace is used. The noise density begins to roll-off at approximately 10 MHz, so for a bandwidth greater than 10 MHz, the V_{RMS} noise estimate is:

$$Magnitude: \quad \left(\frac{50nV}{\sqrt{Hz}} * \sqrt{(f_{bw} - 10\,MHz)}\right) + \left(\frac{205nV}{\sqrt{Hz}} * \sqrt{10\,MHz}\right) \tag{3.15}$$

$$Phase: \quad \left(\frac{45nV}{\sqrt{Hz}} * \sqrt{(f_{bw} - 10\,MHz)}\right) + \left(\frac{225nV}{\sqrt{Hz}} * \sqrt{10\,MHz}\right) \tag{3.16}$$

For a bandwidth less than 10 MHz, only the right half of each equation is used, replacing 10 MHz with the bandwidth:

$$Magnitude: \quad \left(\frac{205nV}{\sqrt{Hz}} * \sqrt{f_{bw}}\right) \tag{3.17}$$

$$Phase: \quad \left(\frac{225nV}{\sqrt{Hz}} * \sqrt{f_{bw}}\right) \tag{3.18}$$

Table 3.4 shows the calculated V_{RMS} and V_{PkPk} noise for different bandwidths, where the V_{PkPk} value is six times the V_{RMS} value, representing six standard deviations.

Table 3.4: Calculated Magnitude/Phase Detector Output Noise

Filter Capacitor (nF)	Bandwidth (kHz)	V_{MAG} RMS Noise (μV)	V_{MAG} PkPk Noise (μV)	V_{PHS} RMS Noise (μV)	V_{PHS} PkPk Noise (μV)
0	32,000	889	5936	923	6094
.1	475	177	1168	194	1282
1	48.2	56.4	372	61.9	408
10	4.82	17.8	117	19.6	129

As expected, as bandwidth decreases, the noise decreases as well. Low noise on the output of the magnitude/phase detector is important to ensure accurate measurements for resonance detection. The experiments performed in this research use a 10 nF capacitor on the filter pin of both the magnitude and phase output of the magnitude/phase detector, unless otherwise noted.

3.7.3 Operational Amplifiers and Analog Controller

The noise of an op-amp is a function of the voltage noise, current noise and resistor noise, and as demonstrated in Table C.2 in Appendix C, the source resistance will determine what noise component will dominate. The figure R_{S-OP} calculates the source resistance at which the dominant noise source will switch from the voltage noise to the current noise [20]:

$$R_{S-OP} = \frac{V_n}{i_n}, \tag{3.19}$$

where V_n is the specified voltage noise density of the device and i_n is the specified current noise density. A higher value of R_{S-OP} allows for higher input source impedances while the voltage still is still the dominant noise source. When the noise is dominated by the current noise, the noise is also a function of the resistance, which is why a lower source resistance is typically preferred.

The amplifiers selected for this design are shown in Table 3.5. The ADA4004-4 amplifier performs the difference, integration, inversion and summation. This amplifier was selected for

its low voltage noise, while maintaining low current noise. As long as an input resistor below 1.5 $k\Omega$, the noise will be dominated by the voltage noise, which is why the source resistors used are 1 $k\Omega$.

The OP270G amplifier is the filter for the signals from the external DAC for V_{BIAS} and V_{HOLD}, as well as the filter between the output of the tracking circuit and the input to the VCO. The OP270G was selected for its low current noise, since the input impedance is higher than seen by the other two amplifiers, at 16 $k\Omega$ for a cutoff frequency of 1 kHz.

The AD8599 is the amplifier used as the buffer before the signal is read into the analog-to-digital converter. The tradeoff between low voltage noise and increased current noise is acceptable in this case because the input impedance is lower than the filter or tracking circuit, as the input impedance is the output of a previous amplifier.

Table 3.5: Calculated Noise Density of Analog Controller Amplifiers

Application	Device	Voltage Noise Density ($nV/\sqrt{Hz}$ at 1 kHz)	Current Noise Density ($pA/\sqrt{Hz}$ at 1 kHz)	R_{s-OP}
Filter	OP270G	3.2	1.1	2.91 $k\Omega$
Controller	ADA4004-4	1.8	1.2	1.5 $k\Omega$
Buffer	AD8599	1.15	2.4	479 Ω

3.8 Tracking Circuit Noise Simulation

The tracking circuit was simulated in Matlab Simulink for both feedback functionality and noise performance by implementing Equation (2.7) and injecting appropriate noise levels at each stage. The noise injected into the system corresponds to the values in Table 3.4, Table 3.5, and Table B.12.

In order to create a proper feedback network for the system to respond to, a one-dimensional interpolation replaces the IDC sensor section of the circuit. The region used for the interpolation is highlighted on top of the IDC sensor frequency response in Figure 3.23.

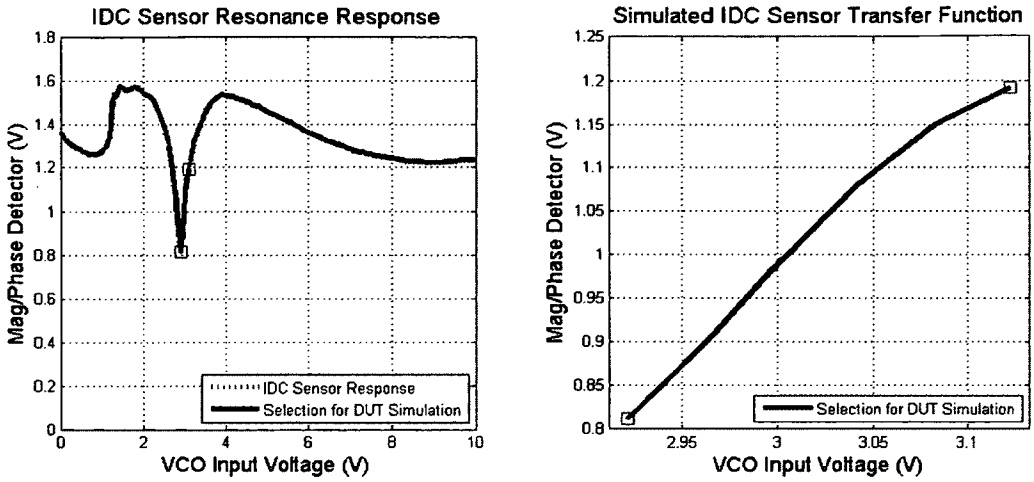


Figure 3.23: IDC Sensor Transfer Function for Simulation

The control point used for the simulation is shown in Table 3.6, and the simulation layout can be found in Appendix D.

Table 3.6: Control Point for Simulation

Parameter	Value (V)
VCO_{BIAS}	3
V_{HOLD}	1

The two figures of merit from the simulation, the noise at the VCO input, and the noise of V_{MEAS}, are shown in Table 3.7. The output shown in Figure 3.24 demonstrates the noise performance from the simulation. In Figure 3.24 through Figure 3.26, the plot of V_{DIFF}, the difference between V_{HOLD} and V_{MEAS}, is shown to demonstrate that the circuit forces the system back to the zero difference state.

Table 3.7: Simulated Noise Results

Signal	1σ	6σ
VCO	0.248 mV	1.49 mV
V_{MEAS}	0.548 mV	3.28 mV

The VCO input is not exactly matched to the V_{BIAS} value of 3 V in Figure 3.24 because the IDC sensor simulated transfer function from Figure 3.23 is not aligned perfectly with the control

point from Table 3.6. The V_{MEAS} signal adjusts to match the V_{HOLD} signal, driving V_{DIFF} to zero, and the circuit compensates for the difference by increasing the input voltage to the VCO. The ability of the system to compensate for these offsets is important for the fabricated circuit, as a DAC cannot generate an exact value with the same precision as a simulated value because of quantization. Adjusting the value of V_{HOLD} to 0.97 V, the VCO input voltage is significantly closer to 3 V, the VCO_{BIAS} voltage, as seen in Figure 3.25.

Figure 3.26 shows the output when a ramp is added to V_{MEAS} to simulate an increasing load applied to the tool causing a resonance shift. As expected, the system responds, forcing the signal V_{MEAS} back to V_{HOLD} by integrating the offset and adjusting the VCO input voltage.

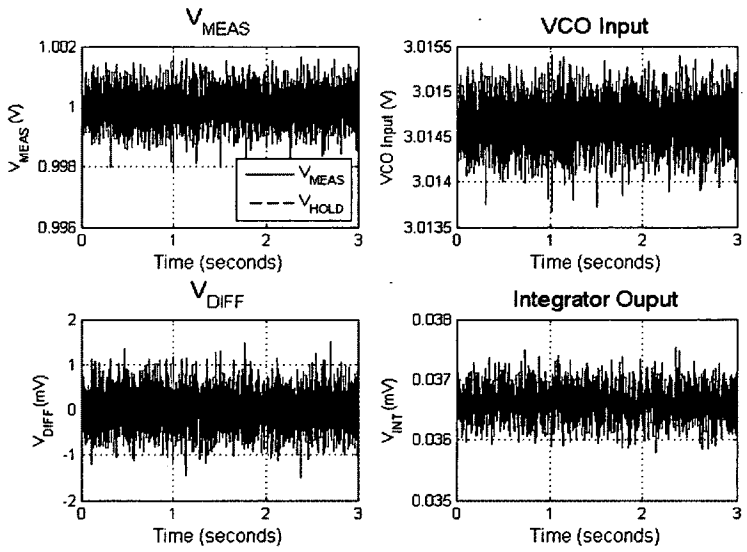


Figure 3.24: Simulated Controller Output Noise

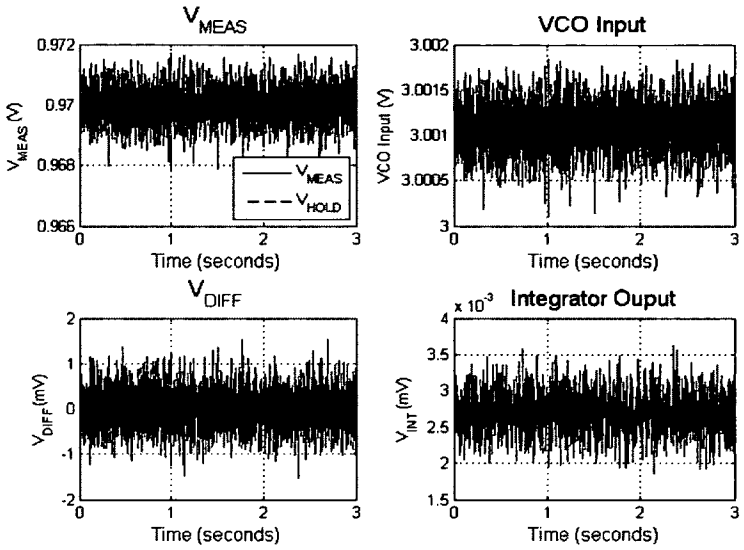


Figure 3.25: Simulated Controller Response, Adjusted V_{HOLD}

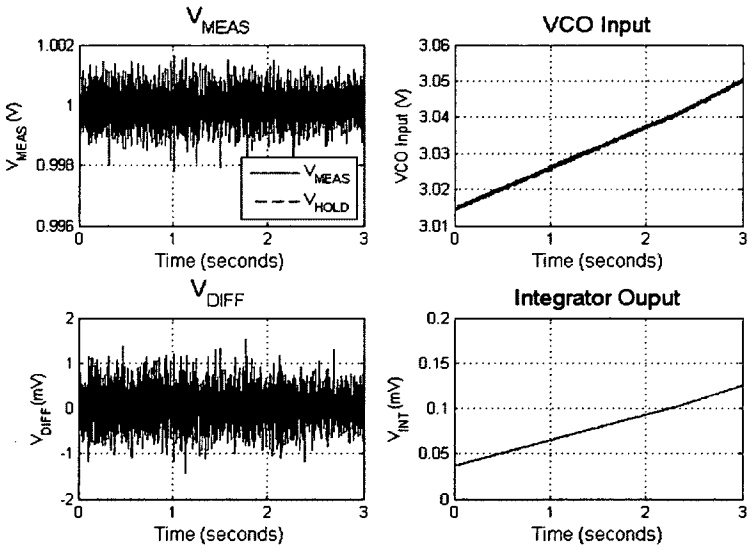


Figure 3.26: Simulated Controller Ramp Response

3.9 Summary

Different types of noise in both the time and frequency domain are presented in this chapter. The noise for both analog and RF circuits is an important factor in the design of a sensitive system. Techniques to quantify the amount of noise to expect in an analog and RF circuit are presented. The noise of an analog circuit is a function of the bandwidth of the

system, and is not determined solely by the manufacturer specification for voltage noise. The current noise of the device is important, and can dominate the total noise if large source resistances are used. Phase noise is the primary concern in an oscillator, causing random fluctuations at the instantaneous output frequency. The system has been modeled to prove it will function as desired, and provides an expectation for noise levels from the fabricated circuit.

In addition, the actual layout and design of the physical circuit board cannot be overlooked, particularly for a two-layer design. Maintaining as close to a full ground plane as possible is important for both the RF and analog circuitry. The ground plane will present a constant impedance transmission line for the RF signal to propagate along, while also allowing high frequency bypass capacitors to via directly to the ground plane to remove any high frequency ripple.

The noise of each component is an important factor in determining the possible resolution of the system. Within the operating range of the DAC and ADC, the higher tuning voltages to the VCO have a lower sensitivity, which would require higher voltage changes for a constant frequency shift. Ultimately, the ability of the ADC to read in the analog voltages is the most important factor. Any improvements to the noise of the system below what the ADC will induce from the measurement will not be reflected in the captured data.

CHAPTER 4

Results

4.1 Introduction

The fabricated circuit as shown in Figure 2.23 was tested for both proper feedback loop functionality and total output noise. This chapter details a statistical analysis of the noise in the captured data and a comparison to the simulated results. Appendix C discusses the standard deviation and the statistics of noise analysis.

4.2 Diagnostic Circuit Noise

To get an understanding of the noise that exists in the RF section of the fabricated circuit, multiple consecutive frequency sweeps were run using the open-loop diagnostic mode of the circuit. Without moving the tool or circuit, 50 sweeps were captured to calculate the standard deviation at each point in the sweep. The standard deviation as a function of frequency shows what parts of the frequency response have the most noise. The experiment was performed for four different experimental setups, and each incremental setup marked an additional layer to decrease the amount of noise in the circuit. For all four experiments, the same FVS5L IDC sensor, which is detailed in Appendix A, was used. Measuring the noise with and without these components demonstrates their effectiveness at reducing noise. For the first experiment, the circuit was populated as shown in Figure 4.1, without an RF shield, filter capacitors or ferrite.

Figure 4.1: PCB Without RF Shield

The second experiment added an RF shield. Figure 3.15 shows the shield without the top cover to show the RF components inside, and Figure 3.16 shows the entire shield. The RF shield is designed to reduce the electromagnetic radiation caused by the VCO, limiting the coupling into the sensor or probe loop.

The third experiment added filter capacitors to the magnitude/phase detector output. Based on the calculated effectiveness of noise reduction for different capacitor values from Table 3.4, 10 nF capacitors were used in this experiment. The final experiment added a piece a ferrite shielding on top of the circuit to absorb electromagnetic radiation, shown in Figure 4.2.

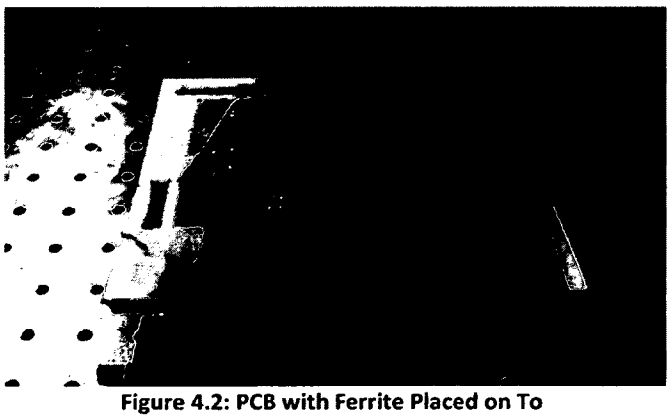


Figure 4.2: PCB with Ferrite Placed on To

The results of all four experiments are shown Figure 4.3. The noise in each experiment is presented as one standard deviation. The measured noise is a function of the entire RF system.

Any noise from the input to the VCO, generated within the VCO, coupled into the IDC sensor, and the noise of the magnitude/phase detector, will all be represented in the results shown in the plot. The plot shows the noise decreasing with each new level of shielding, as expected.

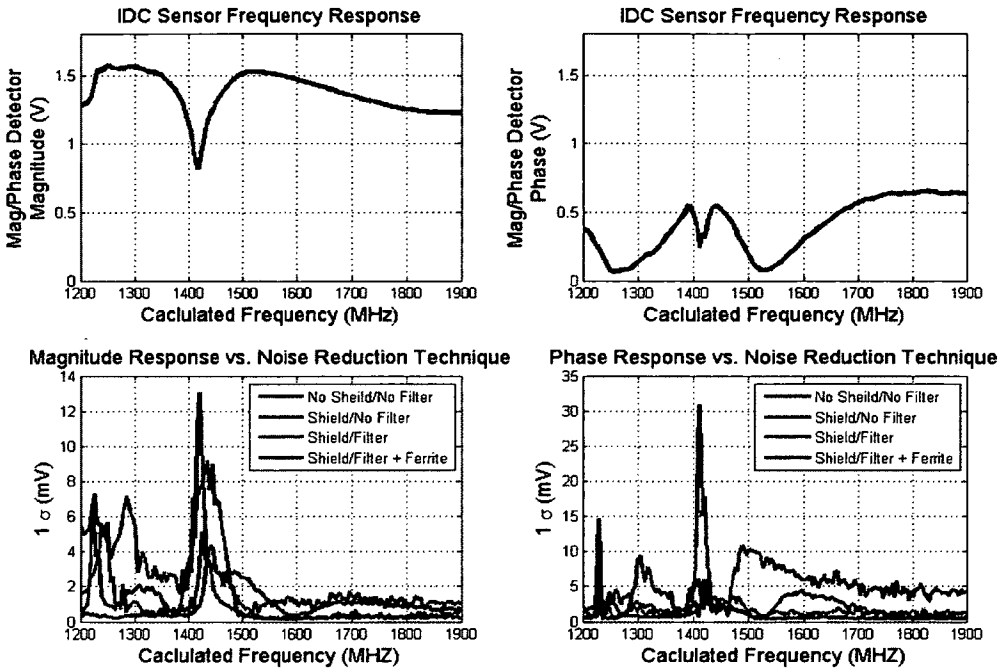


Figure 4.3: Noise of Resonance Response

In Figure 4.3, the noise is the most pronounced at the resonant frequency. The noise at the resonant frequency decreases with each additional technique for noise reduction. The noise is consistently higher on the phase signal, which follows from the higher noise density of the magnitude/phase detector device in Figure 3.22. For the remaining experiments, the experimental setup employs the final technique, which includes the RF shield, 10 nF filter capacitors on the magnitude/phase detector, and ferrite, shown as the purple trace in Figure 4.3, because it has the best noise performance of all the tested methods.

4.3 Experimental Setup

The controller output is directly related to the change in resonant frequency, which contains the information regarding strain. The goal of these experiments was to determine what the

level of noise on the controller output was as compared to the noise required to obtain the desired resolution, and what level of averaging may be required to get the noise down to the desired level.

To measure how the circuit responds to an applied strain on the tool, the Instron machine in the lab, shown in Figure 4.4, was used to apply a known compression force to cause a known strain on the tool. The strain on the tool is calculated from the measured load cell data, and is calculated [5]:

$$\epsilon = V_{load} * \frac{V_{loadSens}}{A * E} \tag{4.1}$$

where ϵ is the strain, V_{load} is the measured voltage output from the load cell, $V_{loadSens}$ is the sensitivity of the load cell at $10\ kN/V$, E is the elastic modulus, Young's modulus, of high strength steel, 207 GPa, and A is the surface area of the end of a 0.5 inch cylindrical tool in square meters:

$$A = \frac{\pi * \left(\frac{1}{2} * 0.0254\right)^2}{4} \tag{4.2}$$

Figure 4.4: Instron Machine in UNH Lab

The machine was set up to perform a compression ramp to bring the tool to a strain of 1000 $\mu\epsilon$. The tool was positioned inside the probe loop, with the circuit position adjusted to match the height of the IDC sensor on the test specimen. Figure 4.5 shows the experimental setup including the Instron machine and mechanical breadboard. The circuit attaches to the mechanical breadboard through three translation tables to allow for minor adjustments in each spatial dimension. Figure 4.6 shows a closer picture of the experimental setup, showing the circuit, test specimen and data acquisition device (DAQ).

Figure 4.5: Experimental Setup for Compression Test

Figure 4.6: Experimental Setup for Compression Test Close-Up

The data was captured at a sampling rate of 10 kHz. The results and conclusions from the data are discussed in the following section.

4.4 Tracking Circuit Results

The goal of the system is to measure strain with resolution of one part in 10^5, which is equivalent to $10\mu\epsilon$. Speed is an important factor in this research, because the machine tool is capable of operating at several thousand RPM. The measurement system must respond quickly to changes in strain to provide the necessary feedback to the machine, and an analysis of the effective sampling rate based on sample averaging is presented below.

The response of the system is described with respect to the change in the resonant frequency due to strain, because the strain directly affects the capacitance of the sensor, causing a change in resonance.

The change in the resonant frequency in response to strain varies with the angle of the sensor with respect to the input and output traces of the probe loop. The convention used in this discussion for the sensor angle is presented in Figure 4.7, where the arrows point to the location of the interdigitated capacitor for each angle, and Figure 4.8 demonstrates the IDC sensor at the 0° position.

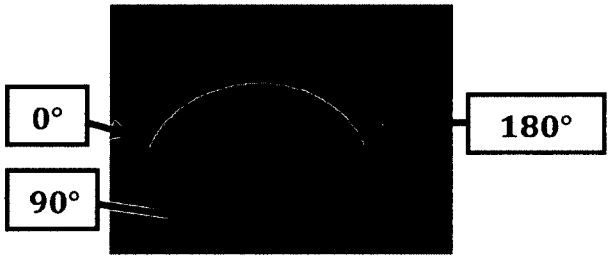


Figure 4.7: Angle of Sensor Rotation with respect to Input and Output Trace Feed

Figure 4.8: IDC Sensor at Rotation Angle 0°

The results in Figure 4.9 are shown normalized to the first data point because the initial resonant frequency was not the same for each test, and the change in resonance is contains the strain information.

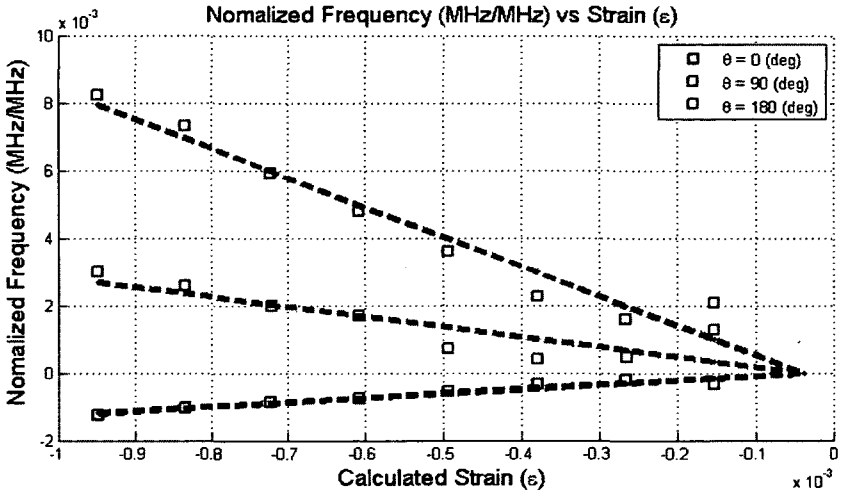


Figure 4.9: Normalized Frequency Shift vs. Strain

The sensitivity of the resonant frequency to strain is calculated from the slope of each trace in the Figure 4.9 as:

$$f_{sens} = \frac{\Delta f_{res}}{\Delta \epsilon}, \tag{4.3}$$

The results for each rotation are show in

Table 4.1, where the total noise of the raw data is represented by f_N and calculated from six standard deviations, and the sensitivity of the resonant frequency to strain is represented by f_{sens}. The magnitude of f_{sens} is used in Table 4.1 to illustrate the differences in the change of the resonance for a given strain at each rotation angle. The cause of the negative slope for the 0 degree angle was not determined and would require further investigation.

If the noise is purely white noise about a constant mean, the noise of the measured signal can be reduced by the square root of the number of samples [21]. To calculate the number of samples required to get the noise down to a desired level, the total noise becomes a function of the square root of the number of samples, N:

$$f_R = \frac{f_N}{\sqrt{N}} \tag{4.4}$$

where f_R is the resolution in terms of frequency. Solving Equation (4.4) for f_R:

$$N = \left(\frac{f_N}{f_R}\right)^2 \quad (4.5)$$

Table 4.1: Sensitivity of Resonant Frequency to Strain for Multiple Sensor Rotation Angles

Rotation Angle	$\lvert f_{sens} \rvert$	f_N	Samples to Average (10 $\mu\epsilon$ Resolution)
0°	1.85 kHz / $\mu\epsilon$	309 kHz	279
90°	12.28 kHz / $\mu\epsilon$	1074 kHz	67
180°	4.33 kHz / $\mu\epsilon$	296 kHz	47

Figure 4.10 shows the three different rotation angles and the effective sampling rate for a measurement with 10 $\mu\epsilon$ resolution. The effective sampling rate is a function of the raw sampling rate and the number of samples required to average to obtain the desired resolution:

$$f_{s-eff} = \frac{f_s}{N^*}, \quad (4.6)$$

where f_{s-eff} is the effective sampling rate, f_s is the sampling rate of the measurement device, and N^* is the number of samples to average. Figure 4.10 also shows the system target sample rate of 100 kHz, and therefore the required sampling rate for each rotation can be inferred at the intersection of this line and the plotted data. As an example, to find the sample rate required for an effective sampling rate of 100 kHz for the 0 degree case, the system must read in data at 28 MHz. The result can also be attained by multiplying the samples to average column from Table 4.1 by the effective sample rate that is desired.

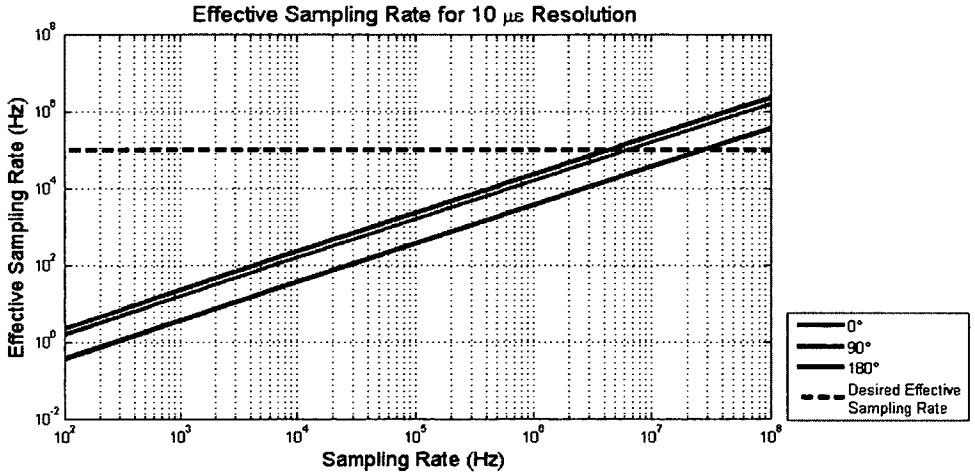


Figure 4.10: Effective Sampling Rate at Different Rotation Angle

If the noise was theoretically reduced, the effective sampling rate would increase because f_N from Equation (4.5) would decrease, therefore requiring less samples to average in order to obtain a strain measurement. Figure 4.11 shows the effect of a reduction in the noise by a factor of 10, 100, and 1000 at the 0 degree rotation angle. For an effective sample rate of 100 kHz and a desired system resolution of 10 $\mu\epsilon$, the effective sampling rate reduces from 28 MHz to 270 kHz for a decrease in noise by a factor of 10, because the number of samples to average is a square function of the noise and resolution.

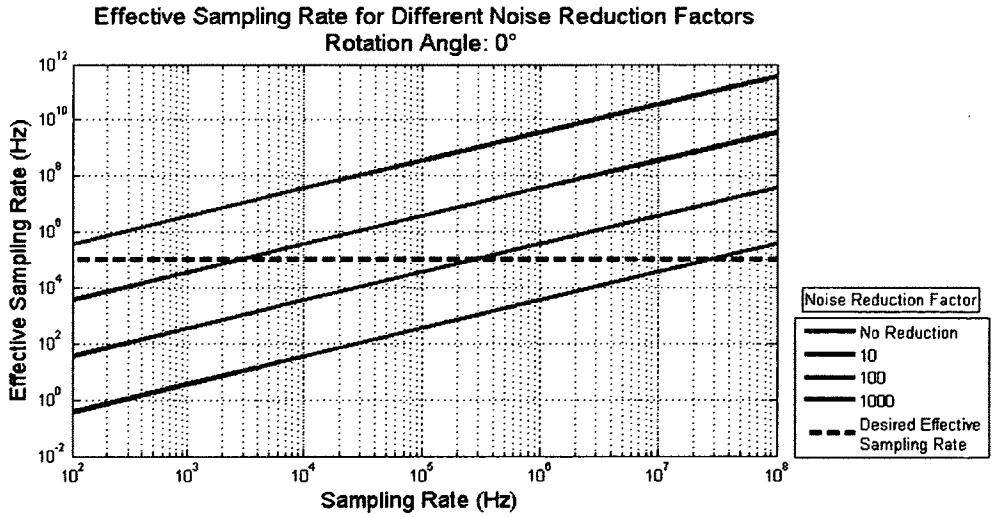


Figure 4.11: Effective Sampling Rate at 0 Deg. for Theoretically Reduced Noise

It must be noted that the results presented in Figure 4.10 and Figure 4.11 do not account for the system response time. The system is limited by the frequency cutoff of the integrator and the low pass filter.

A final experiment was performed to test the step response of the circuit as compared to the model, which can be found in Appendix D. For this experiment, the circuit was used in the closed-loop tracking mode, and a step input adjustment of 20 mV was sent to the V_{HOLD} signal, which is expected to shift the VCO output frequency approximately 1 MHz. The step adjustment causes a non-zero difference at the input to the analog control circuit, and the tuning voltage to the VCO adjusts to compensate for the difference. The plot in Figure 4.12 shows the modeled and measured step responses shifted down to show the VCO output frequency shift, with good correlation between the two. The system bandwidth, as set by the low pass filter, is 1 kHz for both the model and the physical circuit.

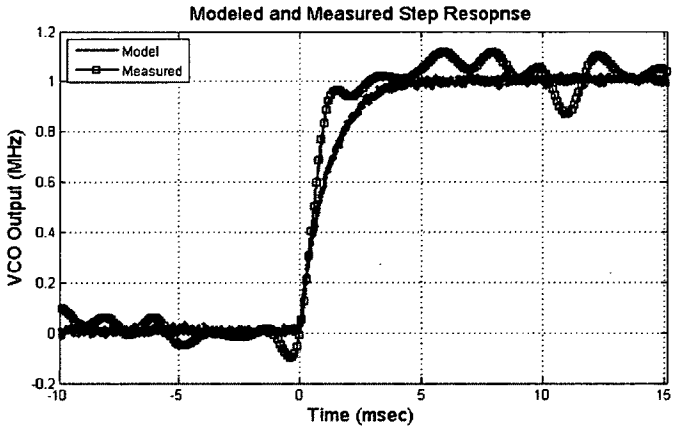


Figure 4.12: Model and Measured System Step Response with Low Pass Filter Bandwidth of 1 kHz

The model has noise injected as described by the manufacturer's specifications for each device in the signal chain. The measured response has a noticeable increase in noise over the modeled response, with the values shown in Table 4.2.

Table 4.2: Modeled and Mesasured Step Response Noise Levels

System	Noise Value
Model	11.2 kHz
Measured	241 kHz

The change in the resonance as a function of the rotation angle across an entire 360° is approximately 17 MHz, and by measuring the time required for the system to settle from a step response, the maximum number of revolutions per minute (RPM) of a machine tool in a CNC milling machine can be calculated:

$$\frac{\Delta f}{\Delta t} = \frac{1MHz}{\Delta t} = f_{slew}\left({}^{MHz}/_{ms}\right) \quad (4.7)$$

$$\frac{f_{rev}}{f_{slew}} = \frac{17\ MHz}{f_{slew}} = t_r\ (sec) \quad (4.8)$$

$$\frac{1\ revolution}{t_r\ seconds} * \frac{60\ seconds}{revolution} = N\ (RPM) \quad (4.9)$$

where Δf is the change in VCO output frequency where 1 MHz is taken from Figure 4.12, Δt is the time required for the system to settle, f_{slew} is the rate at which the output frequency changes, f_{rev} is the 17 MHz frequency shift over one revolution, t_r is the time required to allow the system to fully respond during a revolution, and N is the maximum number of RPM's the measurement system can still respond to. From Figure 4.12, the measured system settles at 10 ms, and the modeled system settles at 5 ms.

Table 4.3: Modeled and Measured Maximum RPM Calculation

System	Maximum RPM
Model	705
Measured	352

If the noise in the model is increased to match the measured system by increasing the noise injected at the VCO input to values consistent with Table 4.1, the result of the model is very similar to the measured data, as seen in Figure 4.13. In this case, the system again settles at approximately 5 ms, but the noise levels are similar to that of the measured data. The higher

noise content obstructs the ability of the system to measure a change such as 18 kHz, which is required for the 10 $\mu\epsilon$ target resolution as shown above in Table 4.1.

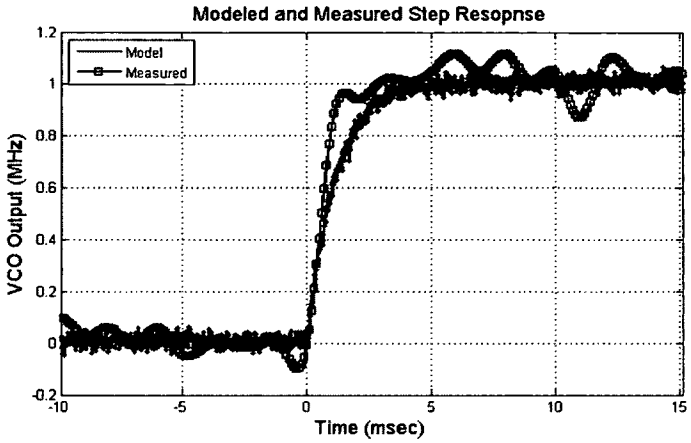


Figure 4.13: Modeled and Measured Step Response with Increased Model Noise, Low Pass Filter Bandwidth of 1 kHz

If the bandwidth of the system is increased in both the model and on the circuit, the noise increases, as shown in Figure 4.14, where the system bandwidth is increased from 1 kHz to 10 kHz. The plot in Figure 4.14 demonstrates that speed of the system response does not increase nearly as dramatically as the noise present in the system. For this reason, further investigation into developing a faster circuit while maintaining low noise is very important to the future of this research.

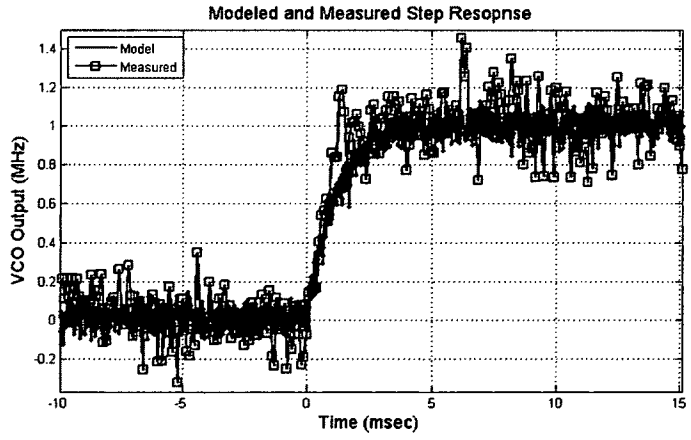


Figure 4.14: Modeled and Measured Step Response with Increased System Bandwidth with Low Pass Filter Bandwidth of 10 kHz

4.5 Conclusion

A means of implementing the circuit to track the changes in the resonant frequency in response to a known strain was presented in this chapter. The noise present in the measurement is the factor that determines the maximum resolution of the system. This chapter presented an analysis of the noise exhibited in the system used in this thesis for multiple rotation angles of the sensor in the probe loop. The analysis also shows the length of time required to perform a measurement based on the desired resolution of the system for a fixed sampling rate. For the goal of $10\mu\epsilon$, the system must average between almost 300 samples for each measurement, assuming the data is normally distributed about a constant mean. For a rotating machine tool, the system would be capable of measuring at a rate of 357 Hz using a 100 kHz measurement device. The analysis concludes with a step response measurement. The step response demonstrates the time required for the system to respond, and the maximum spindle speed rate of a CNC machine is calculated as 705 RPM for the model, and 352 RPM for the physical circuit. The difference between the measured and modeled data is interesting, and further investigation is required to fully understand the characteristics of why this is happening.

CHAPTER 5

Conclusions and Future Work

5.1 Conclusions

The purpose of this research was to develop a method for wirelessly communicating and collecting information from a capacitance-based strain sensor with a target strain resolution of the sensor of one part in 10^5, or 10 $\mu\epsilon$. In order to meet such a goal, a resonant frequency detection and tracking circuit was developed and presented. The noise of the circuit and the system as a whole is critical to resolving such small values. The tracking circuit was simulated using two different simulation packages to test both functionality and performance. The sensor was measured under a compressive loading strain test environment, where the strain was calculated from a load cell.

The simulations showed that the analog circuit operation corresponds to theory, and will be able to track the change in the resonant frequency. The injected noise in the simulation was based on the specified noise metrics from the datasheets of the devices selected for the circuit.

The system sweeps through frequencies from 1 GHz to 2 GHz and measures the relative magnitude and relative phase between a reference and a test channel to find the resonant frequency. The on board tracking circuitry tracks the resonance as it increases or decreases according to strain. For the target set at the beginning of this research of one part in 10^5, or $10\mu\epsilon$, the system must average 300 samples for a measurement while the tool is rotating. The maximum RPM of a machine tool rotating is approximately 350 RPM, based on the speed of the

system step response. Further investigation may lead to improved speed performance without increasing the noise present in the system.

These results demonstrate the successful concept of a system for wireless strain measurement, and with future improvements could replace current techniques and improve manufacturing processes.

5.2 Future Work

For the future of this project, there are a few different approaches and ideas to explore. The design is currently a two-layer PCB that uses an external data acquisition device to perform the analog and digital data conversion. Both of these aspects can be improved upon, as presented below. Another possible improvement for a future design is a different method for generating the RF signal that couples with the IDC sensor. This section discusses how these changes can be implemented in future design revisions.

5.2.1 Multi-Layer Printed Circuit Board

The circuit board used for all the experiments in this thesis is a two-layer PCB manufactured in the lab using a PCB prototyping machine, and moving to a four -layer design could improve the circuit performance. The additional layers could lead to improved noise performance by providing a full ground plane, power plane, and two signal routing layers. The power supply traces to each component would not be on the same layer as the signal traces, and the signal traces would not have to work around the power traces or exist on the ground plane layer. Four-layer designs are the typical minimum in industry, but a two-layer design was implemented in this thesis for decreased development time, as well as the ability to prototype the design in the lab.

5.2.2 Data Conversion

Currently, an external device with 16-bit resolution is utilized for both DAC and ADC conversion. The advantage of this device is its ease of implementation. To move forward with the project, a device that can resolve smaller voltages should be implemented. The problem with implementing a dedicated ADC chip is the engineering trade-offs between resolution and speed, and in this case, ease of implementation since a dedicated ADC would require a redesign of the circuit. As an example, a device such as the ADS1255 from Texas Instruments is capable of reading analog values up to 5 V, with 24-bit resolution at a sample rate configurable up to 30 kHz. For a faster sampling rate, the AD7631 from Analog Devices is capable of 250 kHz sampling rate with 18-bit resolution. Both of these devices provide greater sampling resolution, with a maximum sample rate much higher than used in the final analysis.

To continue using a VCO as the RF signal source, an on-board DAC would eliminate the need for the separate 16-bit external device if the ADC were replaced. The output resolution of the DAC is not as important as its output noise, as it is only providing an initial bias signal for the analog circuit. The output noise of a DAC is not a function of the number of bits of its input, but is defined similarly to an op-amp in units of $nV/\sqrt{Hz}$. The maximum output voltage of a PCB-mounted DAC is typically 5 V or less, and as such, if the resonance measurement of a future sensor requires a VCO voltage higher than 5 V this must be accounted for. The solution could either implement an op-amp in a non-inverting gain-of-two configuration, or identifying a device capable of 10 V output.

Implementing dedicated ADC and DAC devices on the circuit board is another reason to move to a four-layer design, as most manufacturers recommend a four-layer PCB to optimize performance.

5.2.3 RF Signal Generation

Another idea to consider for a future circuit revision is a different RF signal source other than a VCO. The VCO output frequency is generated in an open-loop transfer function based on the input voltage. Below are two different techniques for generating an RF signal.

5.2.4 Phase Locked Loop

A phase-locked-loop (PLL) is an analog feedback system that measures the output frequency of the device and correct for offsets that occur. The output of the device is sent to the load, as well as the feedback input of the device. The measured output is divided by a feedback counter, N, and compared to a lower frequency clock source by a phase frequency detector (PFD). The PFD output will cause an increase or decrease in the voltage to the tuning pin of the VCO, driving the output frequency to the desired value. The feedback increases the accuracy and stability of the output frequency. Analog Devices has several PLLs with and without integrated VCOs, including the ADF4351 with an output frequency range capable of spanning 35 MHz up to 4400 MHz. The output power of the ADF4351 is also programmable between +5 dBm and -4 dBm, removing the need for additional attenuators before the magnitude/phase detector.

5.2.5 Direct Digital Synthesizer

Another technique is to use a Direct Digital Synthesizer (DDS). A DDS uses a time-varying digital signal and performs digital-to-analog conversion to create the final analog output. The advantage of a DDS is very fast output frequency switching and small frequency resolution. Since it is a digital system, the output can be controlled programmatically, providing enhanced flexibility allowing the designer to generate any output frequency on demand or even automatically, depending on the application. The AD9914 from Analog Devices is a very powerful DDS device. The output is controlled by a 32-bit digital word, and can hold an output

frequency up to 1400 MHz with sub-Hz resolution, ramp up, ramp down, and jump to any frequency below 1400 MHz with the only delay between outputs being the propagation delay in the device of less than 1 μsec. The main limitation is the maximum output frequency of 1400 MHz. If another IDC sensor can be used that has a resonant frequency below 1400 MHz, the DDS could provide a good solution.

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Appendix A

Interdigitated Capacitance Sensor

Sensor Design

An interdigitated capacitor does not have two parallel plates like a typical capacitor, but several branches, or fingers, stemming from two opposing sides. The capacitance exists in the area between each finger. The interdigitated capacitor works well in a strain sensing application because the capacitor is only 0.3 mm thick and can easily be adhered to a steel specimen. Figure A.2 shows a close-up of an example sensor with the fingers in a horizontal arrangement. The two large pads on either side are vias that connect to the inductor that wraps around the tool. The vias exist to allow the capacitor itself to be as close to the steel as possible, and the inductor as far away as possible, on the opposite side of the insulation material. An example of an IDC sensor used in this research is shown in Figure 1.7.

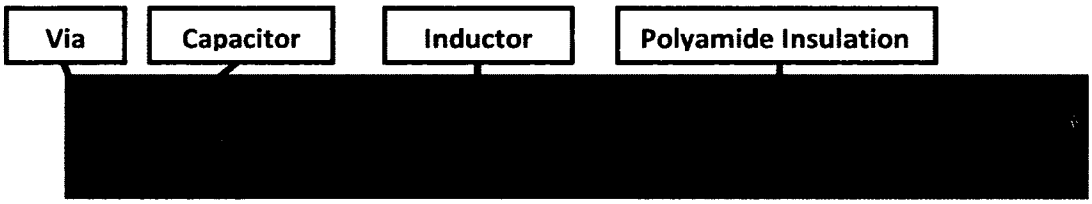


Figure A.1: Example of IDC Sensor used in this Research

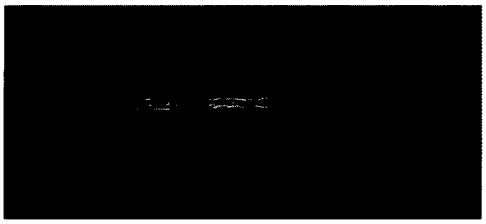


Figure A.2: Close-up of an Interdigitated Capacitor Sensor with Horizontal Finger Arrangement

The sensor shown has a total of 11 fingers, with dimensions of each finger shown in Figure A.3 and listed in Table A.1.

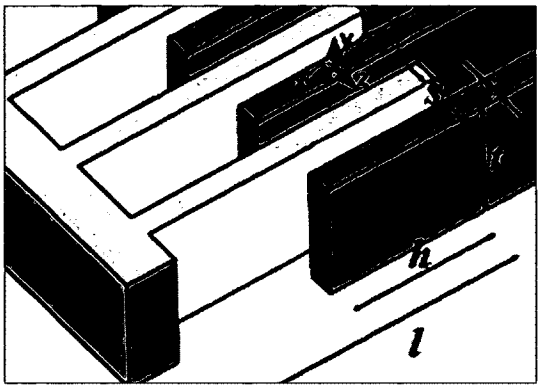


Figure A.3: Dimensions of IDC Sensor Fingers

Table A.1: Dimensions of IDC Sensor Fingers

Finger Dimension	Dimension	Size
Length	l	2.54 mm
Width	w	127 μm
Thickness	t	52μm
Finger Spacing	s	127 μm

Naming Convention

Several different sensors were designed and manufactured previously as a part of this research. The naming convention allows for variations with or without a fixed width between the vias, vertical or horizontal alignment of the fingers, squared off fingers, different number of fingers, and two different finger lengths. The sensor used in this thesis is the FVS5L IDC sensor, where Table A.2 shows what each character represents.

Table A.2: FVS5L Naming Convention

F	**Fixed width:** Width between sensor and vias is fixed
V	**Vertical:** Interdigitated fingers are aligned vertically, opposed to horizontal
S	**Square:** Ends of the interdigitated fingers are square, opposed to rounded
5	**Number of fingers:** $2n + 1 = 11$ total fingers
L	**Long**: The interdigitated fingers are 2.54 mm long as opposed to 1.27 mm

Appendix B

Circuit Component Specifications

RF Circuit

The RF circuit includes the voltage controlled oscillator, the magnitude/phase detector, the RF splitter, and the attenuator. The specifications of each component are detailed below.

Voltage Controlled Oscillator (VCO):

Table B.1: VCO Specifications

Device Part Number	ROS-2230-119+	
Frequency Range (MHz)	**Min**	1064
	Max	2350
Tuning Voltage (V)	**Min**	0.5
	Max	18
DC Power Requirements	**Voltage (V)**	12
	Current (mA)	30
RF Output Power (dBm)	+11	
Phase Noise (dBc/Hz) (at offset frequencies)	**1 kHz**	-70
	10 kHz	-99
	100 kHz	-120
	1 MHz	-141
Non Harmonic Spurious (dBc)	-90	
Frequency Pushing (MHz/V)	0.7	

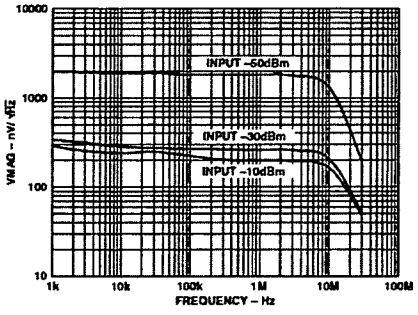
Table B.2: VCO Sensitivity

Voltage Input (V)	Frequency Output (MHz)	Sensitivity (MHz/V)
0.5	1131.3	124
1	1193.4	127
2	1318.2	116
3	1425.2	100
4	1521.3	91
5	1610.3	74
6	1685.9	78
7	1759.2	63
8	1816.8	68
9	1898.3	65
10	1968.1	80

Magnitude/Phase Detector:

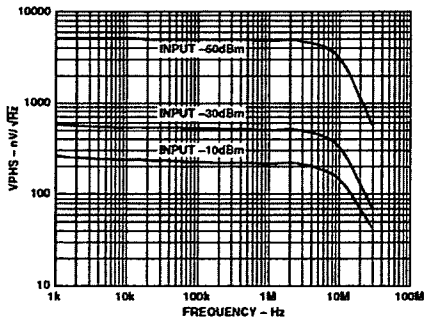
Table B.3: Magnitude/Phase Detector Specifications

Device Part Number	AD8302	
Input Power Range	Minimum RF Power	-60 dBm
	Maximum RF Power	0 dBm
Input Frequency Range	Minimum Frequency	> 0 Hz
	Maximum Frequency	2.7 GHz
Output Voltage Range	Minimum	0 V
	Maximum	1.8 V
Output Sensitivity	Magnitude	30 mV/dB
	Phase	10 mV/Degree



TPC 22. Magnitude Output Noise Spectral Density, $P_{INPA} = P_{INPB} = -10$ dBm, –30 dBm, –50 dBm. No Filter Capacitor

Figure B.1: Magnitude Output Noise Spectral Density



TPC 41. VPHS Output Noise Spectral Density vs. Frequency, $P_{INPA} = -30$ dBm, $P_{INPB} = -10$ dBm, –30 dBm, –50 dBm, and 90° Input Phase Difference

Figure B.2: Phase Output Noise Spectral Density

RF Splitter:

Table B.4: RF Splitter Specifications

Device Part Number	SYPS-2-252+	
Frequency Bandwidth	Minimum	5 MHz
	Maximum	2500 MHz
Insertion Loss	Minimum	3.7 dB
	Maximum	4.4 dB
Phase Unbalance	Maximum	3 Deg.
Amplitude Unbalance	Maximum	0.3 dB

Attenuator:

Table B.5: Attenuator Specifications

Device Part Number	GAT-12+
Nominal Attenuation	12 dB
Frequency Bandwidth	0 Hz to 8 GHz
VSWR	1.15 : 1

Analog Resonance Tracking Circuit

The analog resonance tracking circuit is comprised of multiple operational amplifiers, each with a different purpose. The specifications of each amplifier are shown below.

All of the values in Table B.6 -Table B.8 are from the device datasheet, except the figure R_{S-OP}, which calculates the source resistance at which the dominant noise source will switch from the voltage noise to the current noise [20]:

$$R_{S-OP} = \frac{V_n}{i_n} \tag{B.1}$$

where V_n is the voltage noise density, and i_n is the current noise density of the device.

Controller Amplifier:

This is the amplifier that performs the difference, integration, inversion and summation. This amplifier was selected for its low voltage noise, while maintaining low current noise. As

long as an input resistor below $1.5k\Omega$, the noise will be dominated by the voltage noise, which is why the source resistors used are $1\ k\Omega$.

Table B.6: ADA4004-4 Specifications

Device Part Number	ADA4004-4	
Amplifiers per IC	4	
Maximum Supply Voltage	$\pm 15\ V$	
Supply Current	$2.0\ mA$ per amplifier	
Noise Density	Voltage	$1.8\ nV/\sqrt{Hz}$ @ $1kHz$
	Current	$1.2\ pA/\sqrt{Hz}$ @ $200\ Hz$
Offset Voltage	Typical	$40\ \mu V$
	Maximum	$125\ \mu V$
Slew Rate	$2.7\ V/\mu sec$	
$R_{S\text{-}OP}$	$1.5\ k\Omega$	

Filter Amplifier:

This is the amplifier used to filter the signals from the external DAC for V_{BIAS} and V_{HOLD}, as well as the filter between the output of the tracking circuit and the input to the VCO. The OP270G was selected for its low current noise, since the input impedance is higher than seen by the other two amplifiers.

Table B.7: OP270G Specifications

Device Part Number	OP270G	
Amplifiers per IC	2	
Maximum Supply Voltage	$\pm 15\ V$	
Supply Current	$2.0\ mA$ per amplifier	
Noise Density	Voltage	$3.2\ nV/\sqrt{Hz}$ @ $1kHz$
	Current	$0.7\ pA/\sqrt{Hz}$ @ $100\ Hz$
Offset Voltage	Typical	$50\ \mu V$
	Maximum	$250\ \mu V$
Slew Rate	$2.4\ V/\mu sec$	
$R_{S\text{-}OP}$	$2.91\ k\Omega$	

Buffer Amplifier:

The AD8599 is the amplifier used as the buffer before the signal is read into the analog-to-digital converter. The tradeoff between low voltage noise and increased current noise is acceptable in this case because the input impedance is lower than the filter or tracking circuit.

Table B.8: AD8599 Specifications

Device Part Number	AD8599	
Amplifiers per IC	2	
Maximum Supply Voltage	$\pm 15\ V$	
Supply Current	$4.7\ mA$ per amplifier	
Noise Density	**Voltage**	$1.07 nV/\sqrt{Hz}$ @ $1 kHz$
	Current	$1.5\ pA/\sqrt{Hz}$ @ $1 kHz$
Offset Voltage	**Typical**	$10\ \mu V$
	Maximum	$120\ \mu V$
Slew Rate	$16.8\ V/\mu sec$	
$R_{S\text{-}OP}$	$479\ \Omega$	

Linear Voltage Regulators:

Linear voltage regulators are devices that work to keep a constant output voltage despite changes in the input voltage and load current. The linear regulator maintains a constant output by effectively creating a variable voltage divider between the load the input voltage. The input voltage must always be higher than the desired output voltage, and the power that is not used by the load is dissipated as heat by the regulator.

There are a few key figures to note when selecting a linear voltage regulator. The two most important are the output voltage and output current rating, as the regulator must be capable of sufficiently powering the load. The line regulation is a measure of the device's response to changes in input voltage, and is shown as a change in the output voltage for a given input voltage swing. The load regulation is the device's response to increasing load current. A poorly regulated device will result in a lower output voltage as load current increases. The load

regulation is shown as a change in output voltage for a given increase in load current. The output noise is also important, particularly in this application, as the reason for using a linear voltage regulator is to provide a low noise voltage supply for the amplifiers in the circuit.

The final metric to take note of when selecting a linear voltage regulator is the thermal resistance of the device in the selected IC package. Since a linear voltage regulator is designed to dissipate extra energy as heat, the thermal resistance defines how hot the device will get for a given application. The thermal resistance is provided in units of $°C/W$, which is degrees of temperature increase per Watt dissipated. Most devices have a maximum junction temperature of $125°C$, which is also true of the devices selected in this design. The power dissipated by the device is:

$$P_d = (V_{IN} - V_{OUT})I_{LOAD} + V_{IN} * I_Q \quad \text{(B.2)}$$

where P_d is the power dissipated by the device, V_{IN} is the input voltage, V_{OUT} is the nominal output voltage of the regulator, I_{LOAD} is the total load current seen by the regulator, and I_Q is the quiescent current, or current required for the device to operate.

The junction temperature inside the device:

$$T_J = P_d * \theta_{JA} + T_A \quad \text{(B.3)}$$

where T_J is the temperature of the junction inside the device in $°C$, θ_{JA} is the thermal resistance in $°C/W$ as mentioned above, and T_A is the ambient temperature in $°C$.

If T_J exceeds the maximum temperature of the device, $125°C$, the device will overheat. For smaller device packages such as the SOT-23 used by the LP2985, the thermal resistance is higher than for a package such as the SOIC-8 package used by the LM78L12. The specifications of each linear voltage regulator are shown below in Table B.9 through Table B.11

The $\pm 12\ V$ linear voltage regulators supply power to the operational amplifiers in the circuit.

The $+12V$ regulator also supplies power to the VCO.

Table B.9: +12V Voltage Regulator Specifications

Device Part Number	LM78L12
Output Voltage	+12 V
Maximum Output Current	100 mA
Maximum Input Voltage	+35 V
Line Regulation (14.5 V < V_{IN} < 27 V)	$\Delta V_{out} = 30\ mV$
Load Regulation (1 mA < I_{LOAD} < 100 mA)	$\Delta V_{out} = 30\ mV$
Output Voltage Noise	$80\ \mu V$
Quiescent Current	$3\ mA$
Thermal Resistance	$180°C/W$

Table B.10: -12V Voltage Regulator Specifications

Device Part Number	LM79L12
Output Voltage	-12 V
Maximum Output Current	100 mA
Maximum Input Voltage	-35 V
Line Regulation (-27 V < V_{IN} < -14.5 V)	$\Delta V_{outMAX} = 45\ mV$
Load Regulation (1 mA < I_{LOAD} < 100 mA)	$\Delta V_{outMAX} = 100\ mV$
Output Voltage Noise	$96\ \mu V$
Quiescent Current	$2\ mA$
Thermal Resistance	$180°C/W$

The $+5\ V$ linear voltage regulator powers the magnitude/phase detector, AD8302.

Table B.11: +5V Voltage Regulator Specifications

Device Part Number	LP2985
Output Voltage	+5 V
Maximum Output Current	150 mA
Maximum Input Voltage	+ 16 V
Line Regulation (6 V < V_{IN} < 16 V)	$\Delta V_{out} = 0.7mV$
Load Regulation (1 mA < I_{LOAD} < 150 mA)	$\Delta V_{out} = 12.5\ mV$
Output Voltage Noise	$30\ \mu V$
Quiescent Current	$350\ \mu A$
Thermal Resistance	$220°C/W$

External Data Acquisition Device

The external data acquisition device was the National Instruments NI-6211 USB DAQ. The device has two digital-to-analog convertors (DAC) and eight differential input analog-to-digital convertors (ADC), both of which have 16-bit resolution.

The total full-scale range divided by the number of bits, 2^{16}, determines the bit size. National Instruments uses a calibration technique that uses 5% of the available codes to increase absolute accuracy, which follows the equation:

$$\frac{Input_{MAX} - Input_{MIN}}{2^{16}} * 1.05 \quad \text{(B.4)}$$

There are four available full-scale input ranges for the ADC. The ADC noise is published as one standard deviation in μV_{RMS}, and the peak-to-peak noise was calculated from that as six standard deviations. The bit size, published RMS noise, and calculated peak-to-peak noise are shown in Table B.12.

Table B.12: NI-6211 ADC Device Resolution and Noise

Range (V)	Bin Size (μV)	Noise 1σ (μV_{RMS}) (Published)	Noise 6σ(uV_{PP}) (Calculated)
± 0.2	6.4	12	72
± 1	32	26	156
± 5	160	118	708
± 10	320	229	1374

The DAC output noise was not specified in the device datasheet, but measuring the DAC with the ADC, seen in Table B.13, the noise was consistent with the published ADC specifications. This shows the DAC noise is less than what the ADC can resolve.

Table B.13: NI-6211 DAC Output Measured with NI-6211 ADC

		DAC	ADC	DAC	ADC
Test Output (V)	ADC Input Range (V)	1σ (μV) Measured	1σ (μV) Published	6σ (μV) Measured	6σ (μV) Calculated
2	± 10	246	229	1470	1374
2	± 5	129	118	774	708

Appendix C

Noise Measurement and Calculation

Statistics of Noise

For a signal with a constant mean, normally distributed noise will add to the signal with a known statistical probability. The standard deviation is a statistical tool to evaluate how far a set of data varies from the measured mean, calculated [22]:

$$\sigma = \sqrt{E[(X-\mu)^2]} \tag{C.1}$$

where σ is the standard deviation, X is a random variable, $E[X] = \mu$, and μ is the mean of X. The standard deviation is the root-mean-square (RMS) of the difference between each data point and the mean of the data. The standard deviation does not make sense for data that does not have a constant mean, resulting in an artificially high standard deviation. Figure C.1 shows a set of 1,000 random numbers normally distributed about a mean of zero with a standard deviation of one.

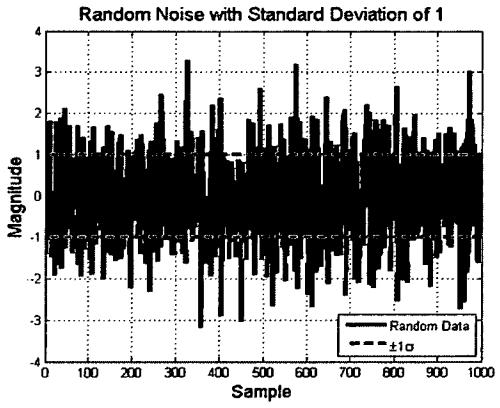


Figure C.1: Standard Deviation of Random Noise

The probability that a measured value will exist within a certain number of standard deviations from the mean is the confidence level. The probability that a measured value is contained within N standard deviations centered about the mean is calculated [22]:

$$P = \mathrm{erf}\left(\frac{N}{\sqrt{2}}\right) \tag{C.2}$$

where P is the probability that the data falls within the confidence interval, and $\mathrm{erf}(x)$ is the error function, defined as [22]:

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}\,dt \tag{C.3}$$

Figure C.2 shows a plot of the probability with increasing confidence interval, and Table C.1 shows the probability for common confidence intervals. For a normally distributed data set, one standard deviation will contain just over 68% of the data, $\pm 34\%$ centered about the mean.

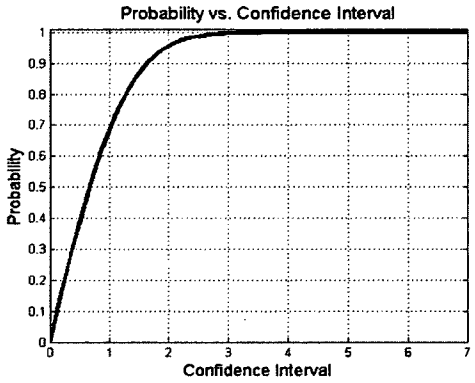


Figure C.2: Probability vs. Increasing Confidence Interval

Table C.1: Confidence Interval Probability

Confidence Interval ($N\sigma$)	Percentage of data within $\pm N\sigma$
1	68.26%
2	95.45%
2.58	99%
3	99.7%
3.3	99.9%

In noise calculations throughout this thesis, a confidence interval of $N = 3\sigma$ is used to obtain a 99.7% likelihood of representing all of the data.

Op Amp Noise Measurement

This section covers the measurement of the noise performance of an operational amplifier. The process is outlined to provide a greater understanding of noise and its impact on op-amps, but was not conducted during this research due to a lack of necessary equipment.

Measurement of the noise capabilities of an op-amp is very important to get an understanding of the total noise to expect in a system. The first step is the selection of the instrument that will make the measurements, for example the HP35670A Dynamic Signal Analyzer (DSA) used by LaFontaine [23]. This instrument will represent the measured signal in $nV/\sqrt{Hz}$ from 0.1 Hz up to over 100 kHz. The noise signal must be amplified by orders of magnitude for the measurement to overcome the noise floor of the instrument. To ensure the signal is above the noise floor without using a large gain on the Device Under Test (DUT), a Post Amplifier (PA) with a known low noise is used with high gain leading into the DSA. The noise can be measured once the signal from the measurement circuit is above the noise floor of the DSA over the full bandwidth of interest. To obtain the actual noise signal, the measured signal is divided by the total gain of the measurement circuit. Figure C.3 shows the noise floor of the DSA device, and the noise of the post amplifier with a gain of 26, and a gain of 101. The gain of 26 does not surpass the noise floor of the DSA at low frequencies, while the gain of 101 is above the noise floor across the full bandwidth of interest [23].

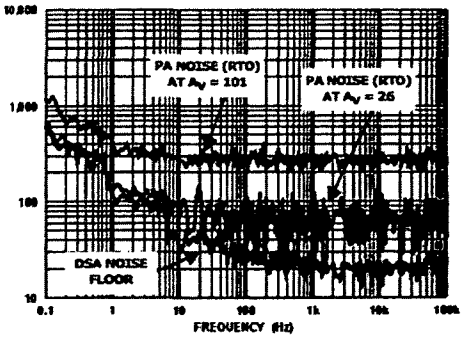


Figure C.3: Noise Floor of DSA vs. Different Post Amplifier Gains

The noise gain is not necessarily the same as the signal gain in a typical op-amp circuit. The non-inverting amplifier gain is always greater than unity, where as the inverting amplifier is theoretically unlimited for either a gain or attenuation.

$$A_{-} = -\frac{R_f}{R_{in}} \tag{C.4}$$

$$A_{+} = 1 + \frac{R_f}{R_{in}} \tag{C.5}$$

Regardless of the op-amp configuration, the noise gain will always be represented by Equation (C.5). The noise gain will now be referred to by A_n where $A_n = A_{+}$.

Figure C.4 shows the circuit schematic for measuring the noise of an op-amp, where A is the total system gain, and AV_n is the noise multiplied by A. DUT is the device under test, and PA is the post amplifier before the DSA.

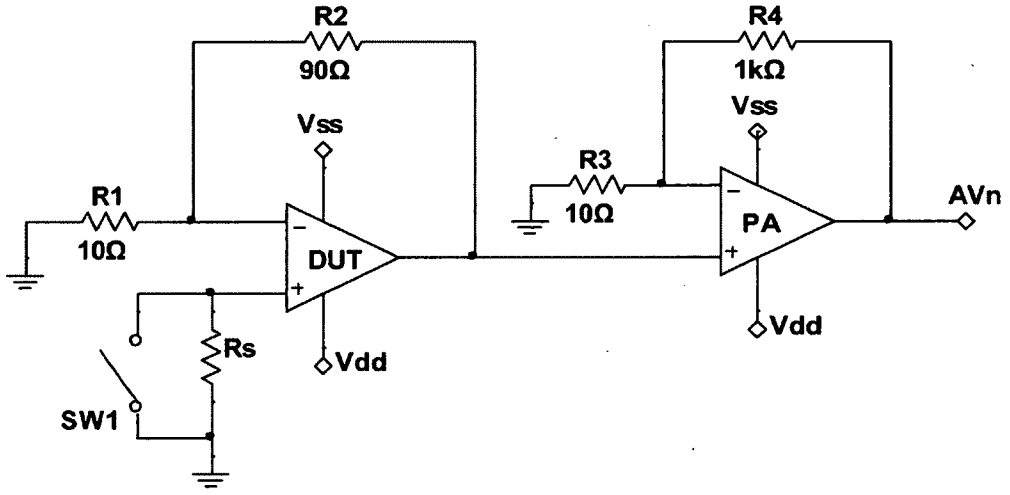


Figure C.4: Circuit Schematic for Op-Amp Noise Measurement

$$AV_n = (A_{DUT})(A_{PA})(V_n) = \left(1 + \frac{R_2}{R_1}\right)\left(1 + \frac{R_4}{R_3}\right)(V_n) = 1010 * V_n \tag{C.6}$$

The switch SW1 is closed for voltage noise measurements, shorting out the resistor R_S to prevent any current from flowing through it. The switch is open for current noise measurement,

forcing the current to flow through the resistor and generate a proportional voltage noise. The current noise is measured by the voltage noise created across the known resistance R_S.

As the source resistance increases, the noise generated by the resistor itself will begin to overtake a low voltage noise device. For applications with high source impedance, choosing an op-amp with a very low current noise is the most important factor, as the voltage created across the source resistor will dominate the other noise sources. It should be noted that the source resistance is not always explicitly a resistor, but may be the output impedance of the previous stage in a circuit.

Calculating Total Noise in Op-Amp Circuit

The total noise of the system can be calculated from the value V_n measured via the technique described above. The voltage noise can be modeled as a voltage source in series with the input to an ideal op-amp. The noise specified by a manufacturer is referred to the input (RTI), which allows the designer to find the noise referred to the output (RTO) for any configuration and gain. Figure C.5 shows the schematic of an ideal op-amp with all six noise sources, the voltage noise,V_n, the current noise at each input terminal named for the resistor it flows through, I_{n1} and I_{nS}, and the Johnson noise of each resistor, V_{nRx}, where x represents the resistor.

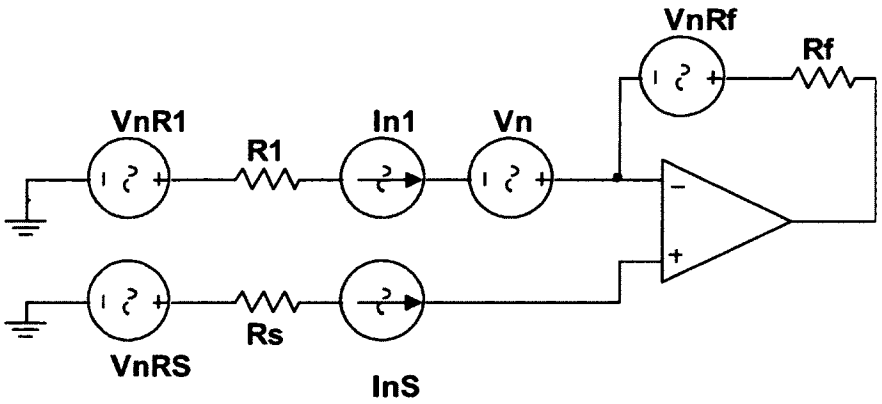


Figure C.5: Schematic of Ideal Op-Amp with All Noise Sources

The specified voltage noise, as well as the voltage noise created by the current noise across the input resistors, and Johnson noise of the input resistors, are all affected by the noise gain. Of the three types of noise sources, the voltage source, current source, and resistor, any of the three could dominate the noise at the output. The source resistance plays a large part in the dominating noise source, as it allows the current noise to create a voltage. The effect of different source resistances is shown in Table C.2 as an example for a voltage noise $V_n = 5\ nV/\sqrt{Hz}$ and current noise $I_n = 1\ pA/\sqrt{Hz}$. The current noise is multiplied by the source resistance so all three values are represented in $nV/\sqrt{Hz}$ for comparison. The bandwidth is not important to determine which source will dominate, as multiplying by the square root of the bandwidth would not change the ratio of the values. Table C.2 shows that for different source resistances, any of the three noise sources can dominate, depending on the specified values of V_n and i_n.

Table C.2: Calculated Noise vs. Source Resistance

Noise Source	Source Resistor (R_S)		
	0Ω	**5kΩ**	**50kΩ**
Johnson Noise of R_S	0	**9.1**	28.7
Current Noise ($1pA/\sqrt{Hz}$) * R_S	0	5	**50**
Voltage Noise ($5nV/\sqrt{Hz}$)	**5**	5	5

The device datasheet should also have a plot similar to Figure C.6, showing the voltage and current spectral noise density for that device. For the device represented in Figure C.6, the 1/f corner frequency is approximately 100 Hz for both the current noise and voltage noise.

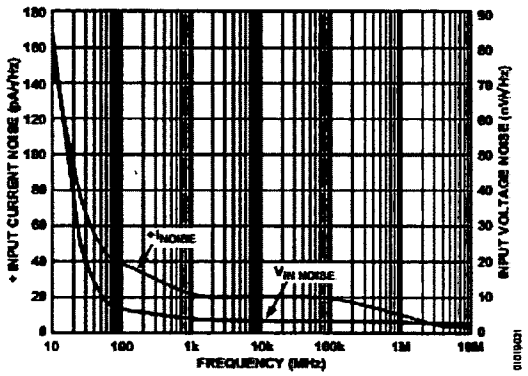


Figure C.6: Voltage and Current Noise Spectral Density for AD8016

For applications that will have a very small bandwidth, the op-amps datasheet will usually have a separate specification for the pink noise, or 1/f noise, over a specified bandwidth. This value is listed in the datasheet as a peak-to-peak voltage because the bandwidth is already defined.

Noise sources combine as a function of their respective signal power. When working with noise in terms of voltages, the noise sources combine as the square root of the sum of the squares as shown in Equation (C.7).

$$V_{TOT} = \sqrt{V_1^2 + V_2^2 + V_3^2} \qquad \text{(C.7)}$$

The total output noise, N_S, as a function of the system bandwidth, derived from the schematic in Figure C.5 is:

$$N_S = \sqrt{(V_n^2 * A_n) + ((I_{n1} * R_f)^2 * A_n) + ((I_{nS} * R_s)^2 * A_n) + \left(J_1 * \left(-\frac{R_f}{R_1}\right) * A_n\right) + (J_S * A_n) + J_f} \qquad \text{(C.8)}$$

where each variable is defined in Table C.3.

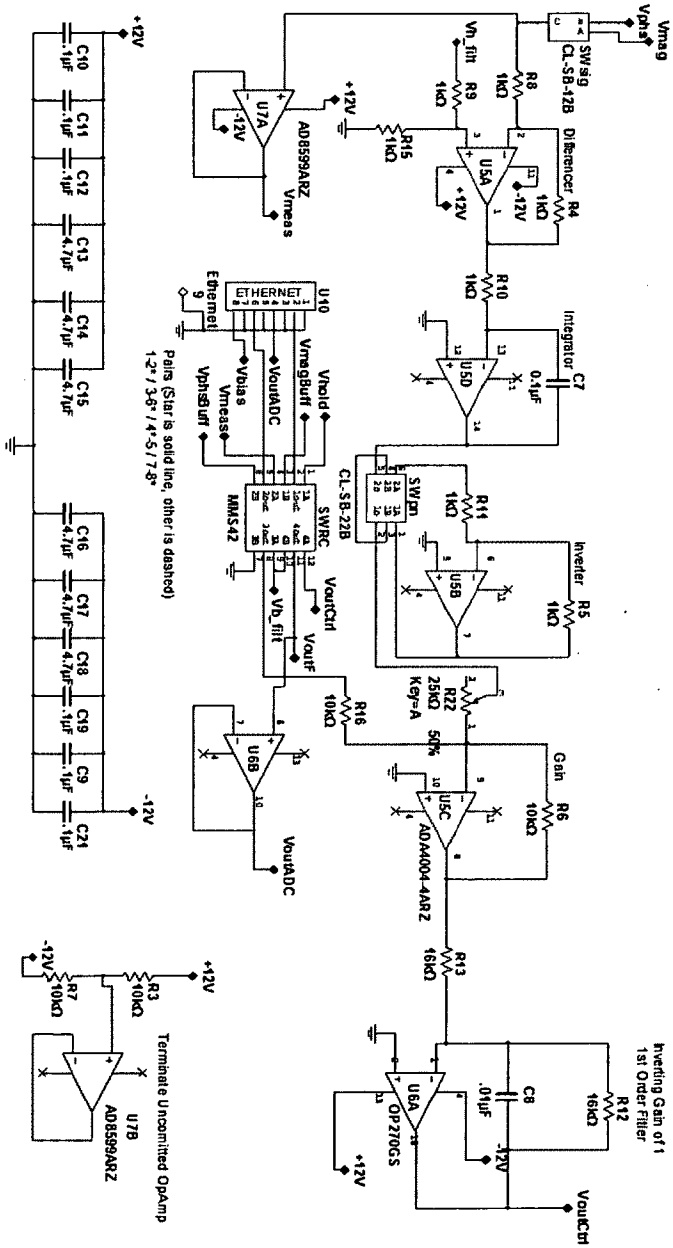
Table C.3: Variable Definitions for Equation (C.8)

Variable	Definition
V_n	Voltage Noise per $\sqrt{Hz}$
A_n	Noise Gain
I_{n1}	Current Noise per $\sqrt{Hz}$ through R_1
I_{nS}	Current Noise per $\sqrt{Hz}$ through R_s
J_1, J_s, J_f	Johnson Noise of Each Resistor

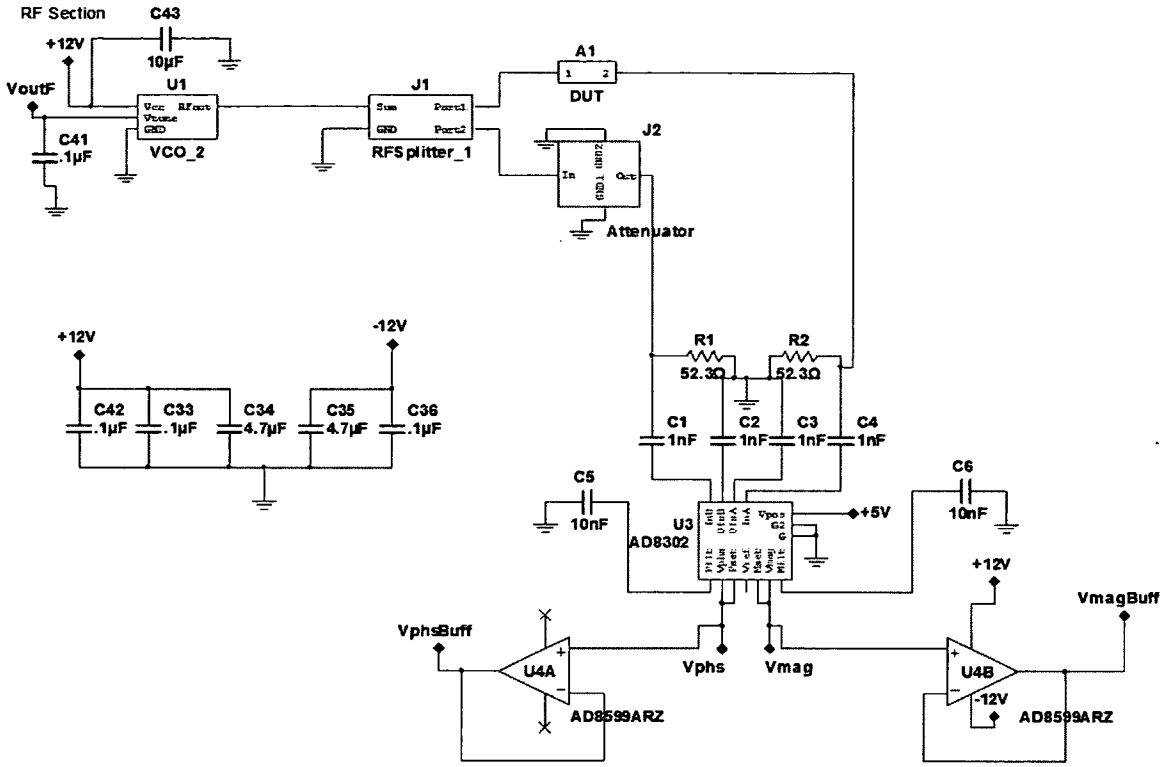
Appendix D

Circuit Schematic and Layout

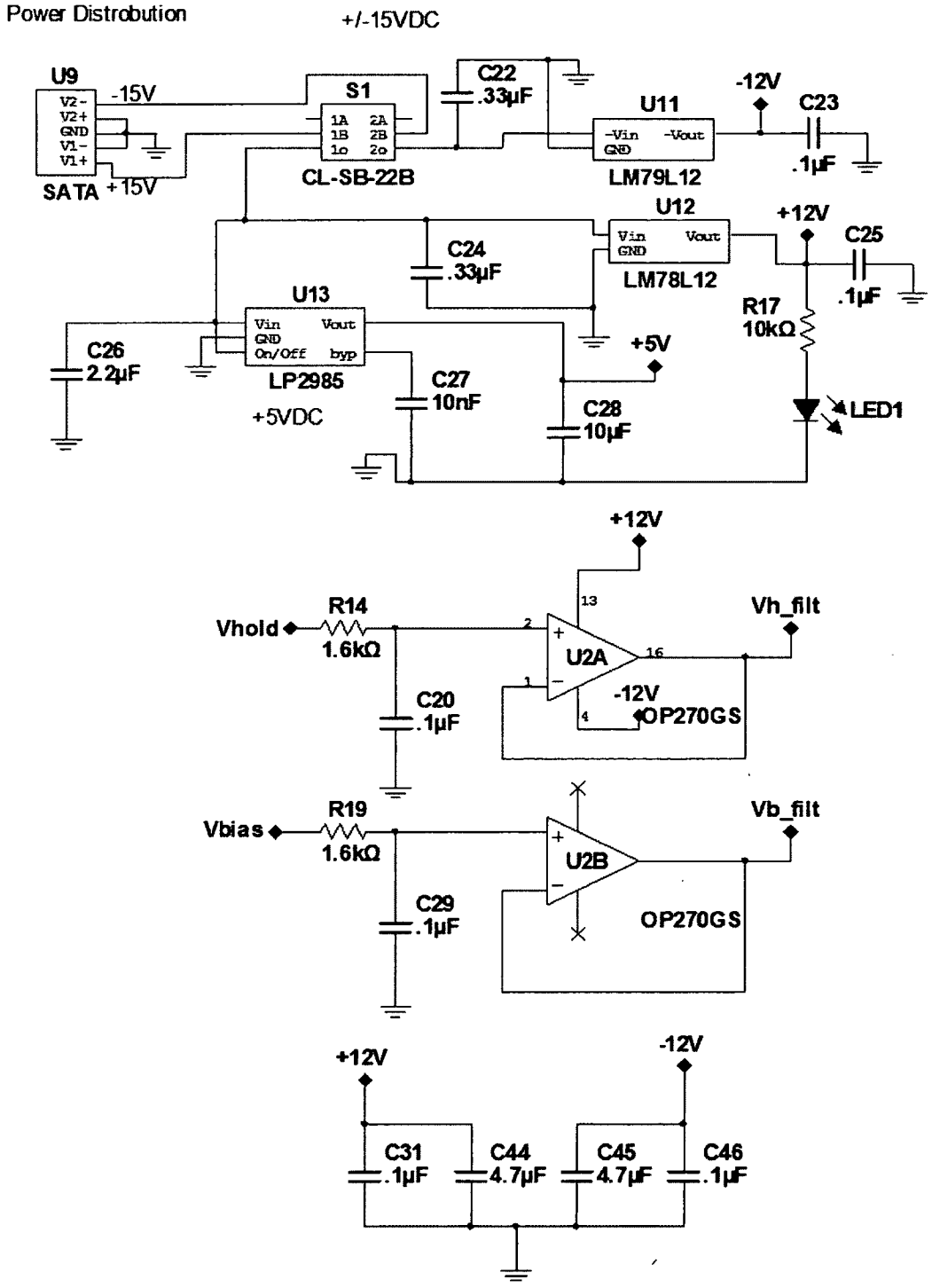
Schematic – Analog Controller



Schematic – RF Circuit



Schematic – Power Distribution and Voltage Input



PCB Layout – Top Layer

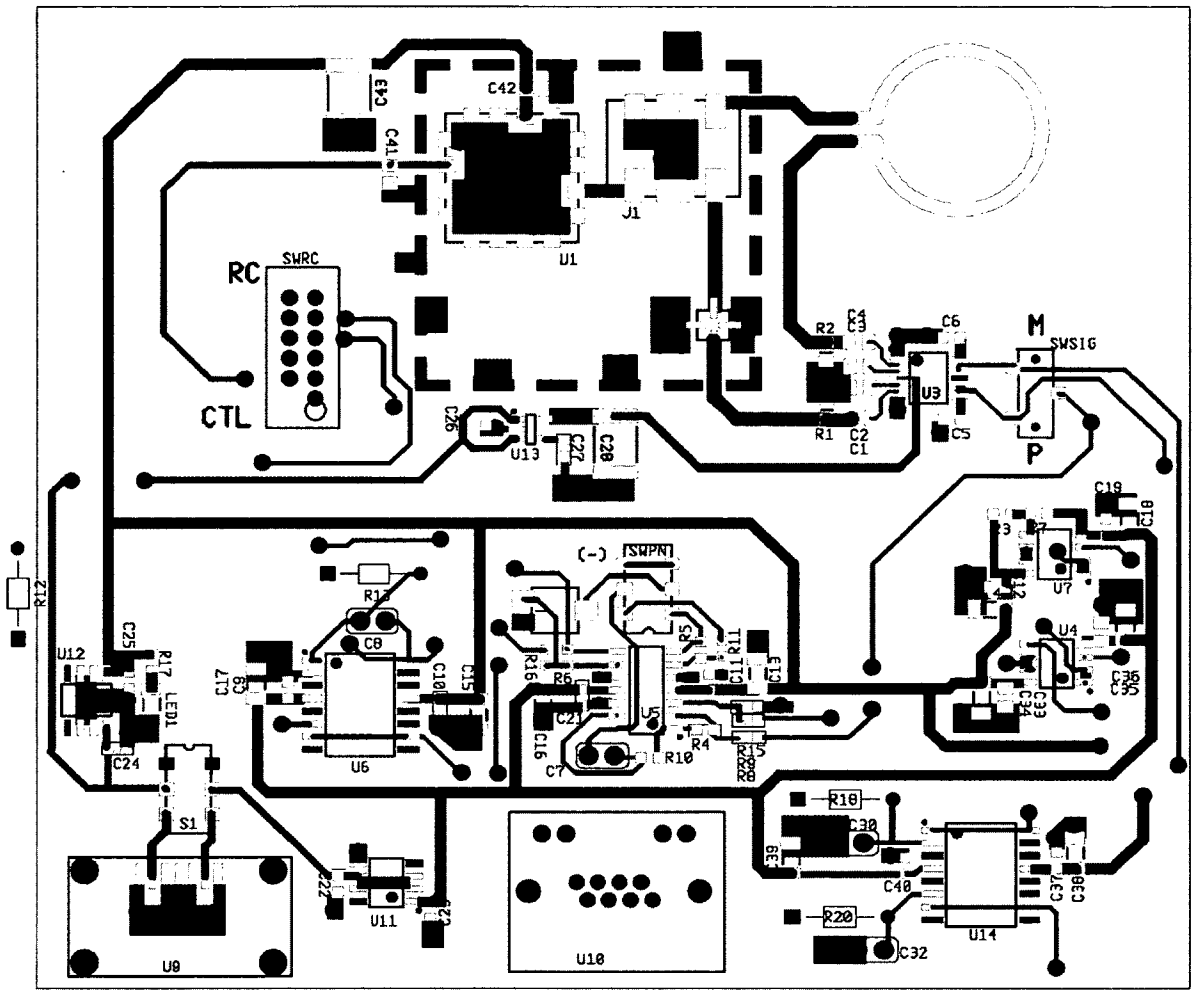


Figure D.1: Top Layer PCB Layout and Routing

[1] Resistor R_{12} is shown off the board because it was added after fabrication. It connects to pin 1 and pin 16 on device U6.

PCB Layout – Bottom Layer

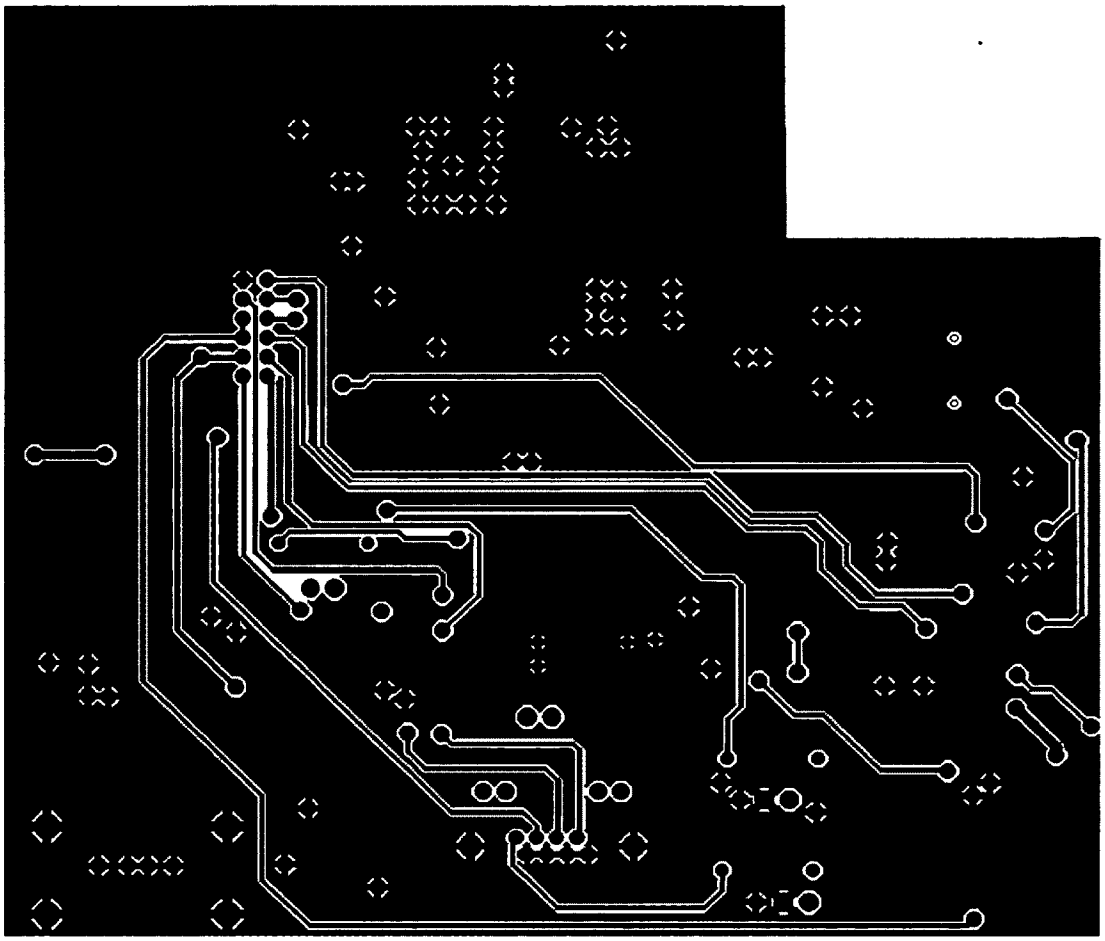


Figure D.2: Bottom Layer PCB Layout and Routing

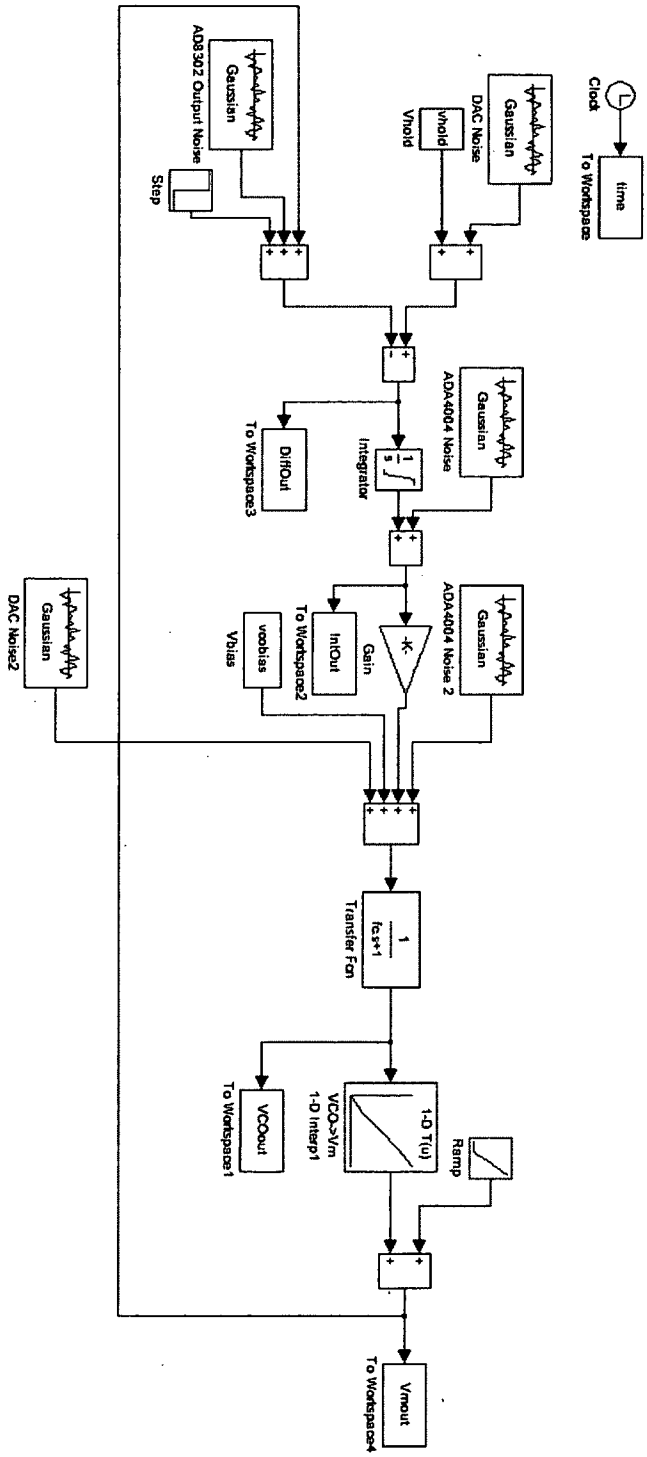
Component List

The components in the design are listed in Table D.1 according to their layout designation number in the PCB Layout from Figure D.1.

Table D.1: List of Components from PCB Layout

Layout Designation	Part	Description
J1	SYPS-2-252	RF Splitter
S1	Switch	Power Switch
SwPN	Switch	Pos./Neg. Slope Switch
SwRC	Switch	Resonance/Control Switch
SwSIG	Switch	Magnitude/Phase Control Switch
U1	ROS-2230	Voltage Controlled Oscillator
U3	AD8302	Magnitude/Phase Detector
U4	AD8599	Buffer
U5	ADA4004-4	Controller Op-Amp
U6	OP270GS	Filter Op-Amp
U7	AD8599	Buffer
U9	eSATA	Power Jack
U10	RJ-45	Ethernet Jack for Data
U11	LM79L12	-12V LDO
U12	LM78L12	+12V LDO
U13	LP2985	+5V LDO
U14	OP270GS	Input Filter Op-Amp

Matlab Simulink Model



Appendix E

LabVIEW and Matlab Software

LabVIEW Software

The software that interfaces with the circuit is written in LabVIEW, utilizing the built-in functionality to directly communicate with the data acquisition device (DAQ). The "Capture Mode" drop down box allows the user to select either "Resonance Curve" or "Control", and the software measures the data with the DAQ and writes the data to an appropriate file. The file is titled "Circuit_v2.vi".

Resonance Curve:

The front panel for capturing a resonance curve is shown in Figure E.1. Upon running the code for resonance capture, the plots on the front panel will automatically update with each read sample until the sweep has completed.

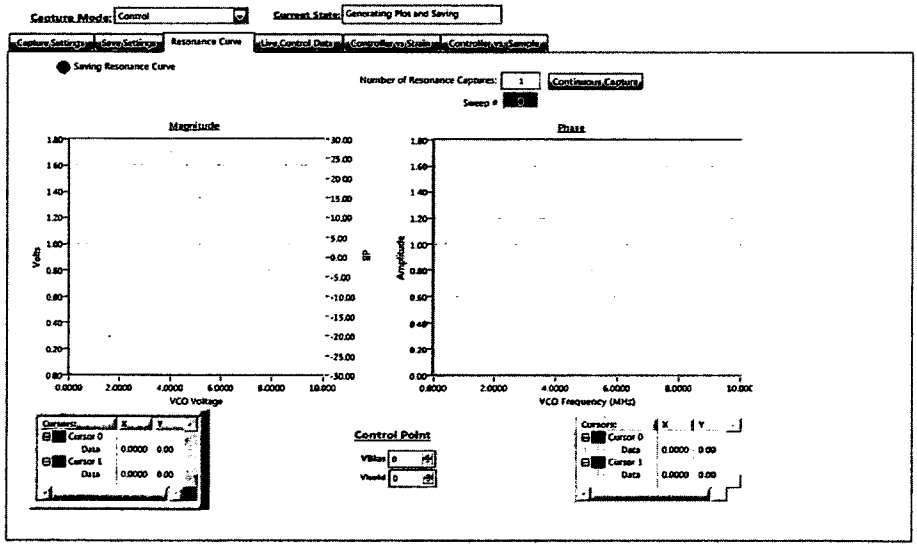


Figure E.1: "Resonance Curve" Panel for LabVIEW Circuit_v2.vi Software

Control Data:

To capture control data, which contains the strain information in the input voltage to the VCO, set the "Capture Mode" drop down menu to "Control". The top plot in the front panel, shown in Figure E.2, displays a live update of the measured control signal to the VCO, and the bottom plot displays a live update of the measured voltage out of the magnitude/phase detector. Operating the software in this mode allows the user to view changes in real-time, helpful for confirming the controller is working properly. To capture a set of control data, click the "Collect Control vs. Strain Data" button at the top, and the software will immediately begin sampling data using the external DAQ with the sample rate and number of samples that are set in the "Capture Settings" panel. The software may appear to stop responding, but the front panel is not updated until the sampling process completes. The "Current Status" indicator at the top will change to "Generating Plots and Saving" after sampling has completed, and the front panel window will automatically switch to the "Controller vs. Strain" tab to display the measured data.

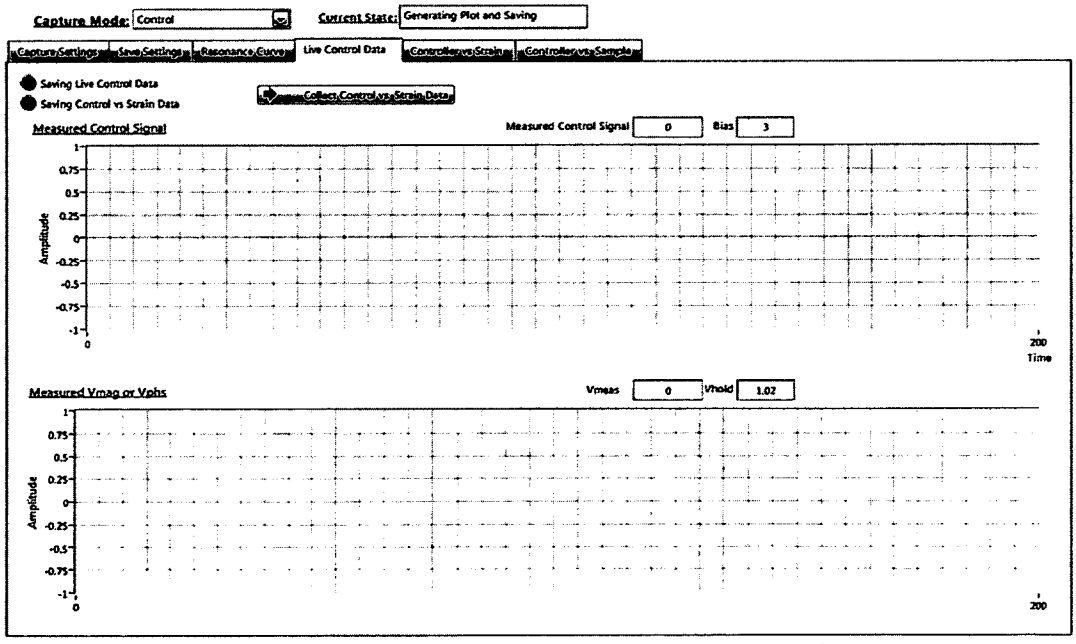


Figure E.2: "Control Data" Panel for LabVIEW Circuit_v2.vi Software

Save Setup:

The "Save Settings" panel allows the user to set the main path where the files will be saved, the name of the folder in which to save the following tests in, and the name of each file. The file name entry must contain 'RC' somewhere in the filename for resonance data in order for the Matlab post processing code to distinguish between resonance and control files. There is no corresponding requirement for control file names. Appending "00" or "_00" to the end of the file name is recommended, because the software will automatically increment the filename to "x_01", "x_02", as files are saved into the same directory. Information about the control signal, such as the V_{BIAS} voltage and V_{HOLD} voltage, is automatically saved into the comment section of the control data file and read by the Matlab post processing code. Additional comments can be added in the "Additional Comments in Control File" box. The "Save Settings" panel is shown in Figure E.3.

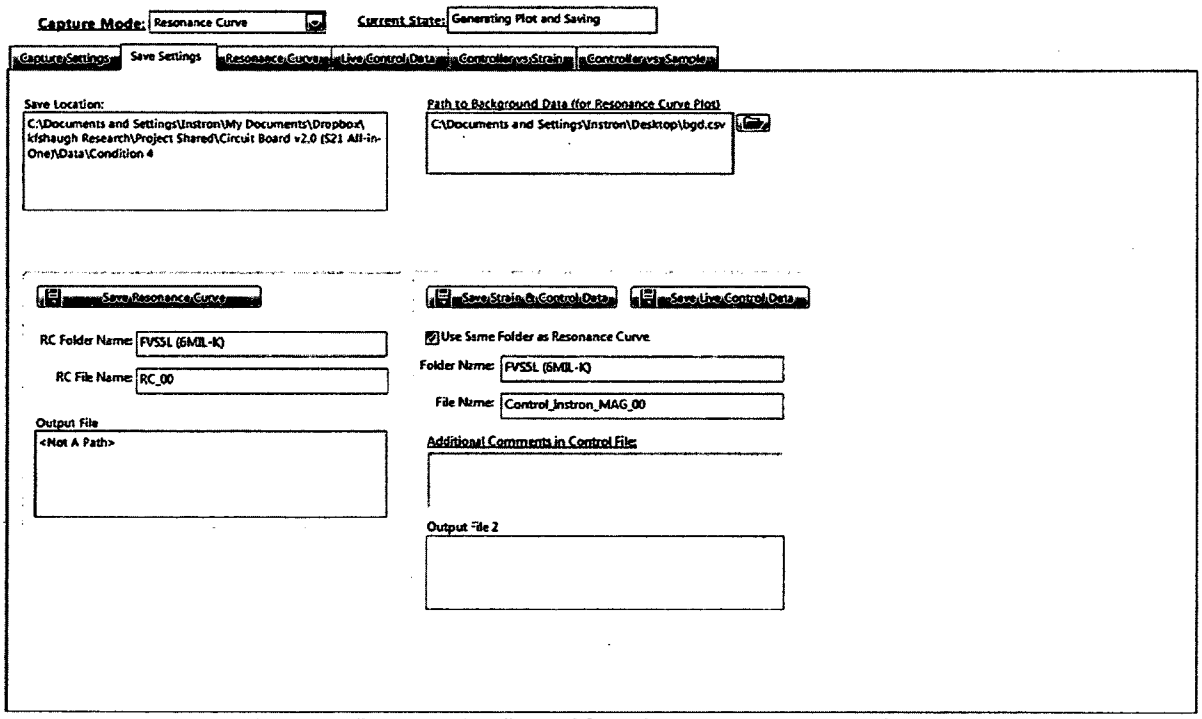


Figure E.3: "Save Settings" Panel for LabVIEW Circuit_v2.vi Software

Matlab Code

The import data function `ctl_import()` is the Matlab code to import the data captured with the LabVIEW software "Circuit_v2.vi" for analysis. Calling the function by specifying three output arguments, without input arguments:

```
[rc ctl testname] = ctl_import();
```

prompts the user to select a folder that contains the files to be analyzed. All of the LabVIEW measurement files (files with the extension `.lvm`) within the selected folder are imported; any other file formats and subfolders are ignored. It reads files for both resonance data and control data. The function automatically considers the data file a resonance file if the string `'RC'` exists anywhere in the filename; otherwise the file is read in as a control data file. Each data file contains multiple sections of information, and each file is imported into a structure cell array named either `rc` or `ctl` according to the example above, to aid in analysis and plotting. The folder name selected by the user in the prompt is stored in `testname`.

As an example to illustrate the data format, if there are three resonance data files in the selected folder, the magnitude data of each file is accessed:

```
rc.mag{x,1}
```

where `rc` is the structure containing all resonance data, `.mag` selects the structure element containing the magnitude data of all three files, and `{x,1}` accesses the cell that corresponds to resonance file "x". So, `rc.mag{2,1}` selects the magnitude data of the second resonance file in the selected directory.

The function also allows the user to apply a zero-phase forward and reverse filter, implemented with the Matlab built-in `filtfilt()` function by specifying input arguments 'filt' and Order as:

```
[rc ctl testname] = ctl_import('filt',1000)
```

which will apply a 1000 order filter to the control data for the measured VCO input voltage, calculated VCO output frequency, and measured output voltage of the magnitude/phase detector, saved with "_f" concatenated to the structure element to preserve the raw data. (i.e. `ctl.vcov_f{x,1}` for the filtered measured VCO input voltage.)

The `lvm_import()` function that is called within this function to perform the actual read and import from the LVM file was written by M. A. Hopcroft and is publicly available on the Matlab File Exchange on the Mathworks website, last updated on May 31, 2012.

```
function [rc, ctl, testname] = ctl_import(StringIn,order)
%CTL_IMPORT prompts user for a folder containing CONTROL or RESONANCE
%data files and imports them into appropriate structures.
%
%[rc ctl testname] = ctl_import() imports any CONTROL and RESONANCE
data
%files within the selected directory. The data can be accessed as
follows:
%
%RESONANCE data is saved:
%rc.mag{x,1} = magnitude data from resonance curve
%rc.phs{x,1} = phase data from resonance curve
%rc.vcov{x,1} = VCO input voltage
%rc.vcof{x,1} = VCO output frequency from transfer function of
"volt2freq"
%rc.name{x,1} = name of resoance curve file
%
%where x refers to the "x"th RESONANCE file that was read in
%EXMAPLE:
%plot(rc.vcof{2,1},rc.mag{2,1}) will plot the MAGNITUDE data vs.
FREQUENCY for the second RESONANCE FILE read in from the directory
%
%CONTROL data:
%ctl.vcov{x,1} = Input voltage to VCO
%ctl.vcof{x,1} = Output frequency of VCO
%ctl.vm{x,1} = Measured voltage of AD8302 (Magnitude or Phase)
%ctl.strain{x,1} = Calculated Strain based on load cell data of Instron
%ctl.vbais{x,1} = Bias votlage of VCO
%ctl.vhold{x,1} = Bias voltage of AD8302
%ctl.name{x,1} = name of control data file
%
%where x refers to the "x"th CONTROL file that was read in
%EXMAPLE:
%plot(ctl.strain{2,1},ctl.vcof{2,1}) will plot the calculated STRAIN
%vs. the output FREQUENCY of the VCO for the second CONTROL FILE read
%in.
%
%If folder contains no RC or CTL data, the respective variable will
```

```
%result in "NaN".
%
%testname = Name of folder selected
%
%FILTER:
%The data can be filtered if desired, and is saved with "_f" at the end
%of each variable that was filtered.
%
%[rc ctl testname] = ctl_import('filt',ORDER) applies filtering, based
%on the order set by ORDER. Filter is a matlab filtfilt zero-phase,
%forward and reverse filter.  Using 'filter' in place of 'filt' works
%as well.
%EXAMPLE:
%[rc ctl testname] = ctl_import('filt',100);
%ctl.vcov_f{x,1} is the filtered version of ctl.vcov{x,1}, with a 100
%Order filter
%
%Non-data files (files that are not *.lvm) are ignored.
%Subfolders within the directory are also ignored.
%Chris Dean, 2013
if nargin == 1
   error('filt specified without filter order');
end
rc_count = 1;
ctl_count = 1;
Area = (pi*(0.5*25.4e-3)^2)/4;      %Area of 0.5inch cylinder edge
E = 207e9;                    %young's modulus for high strength steel

foldername = uigetdir;        % Opens Dialog to select folder where data
is saved
files = dir(foldername);files = files(3:end);   %grabs all files within
selected folder
d = cell(length(files),1);     %pre-allocate memory for import
% Import
for i=1:length(files)
 if ~files(i,1).isdir                              %If not a folder
  if strcmp(files(i,1).name(end-3:end),'.lvm') %If LVM file
   if (files(i,1).bytes>0)                         %If file is not empty
    fprintf(['Loading File #%d of ' num2str(length(files)) char(10)
files(i,1).name '\n'],i);
     d{i,1} = lvm_import(fullfile(foldername,files(i,1).name),0);
       if isempty(regexp(files(i,1).name,'RC','once'))
           % Allocate Control Data
           ctl.vcov{ctl_count,1} = d{i,1}.Segment1.data(:,2);
           ctl.vcof{ctl_count,1} = d{i,1}.Segment1.data(:,3);
           ctl.vm{ctl_count,1} = d{i,1}.Segment1.data(:,1);
           ctl.load{ctl_count,1} = d{i,1}.Segment1.data(:,4);
           ctl.strain{ctl_count,1} =
ctl.load{ctl_count,1}*10e3/(Area*E);
           ctl.name{ctl_count,1} = files(i,1).name;
           ctl.comment{ctl_count,1} =
regexp(d{i,1}.Segment1.Comment,';','split');
           ctl.vbias{ctl_count,1} =
str2double(ctl.comment{ctl_count,1}{1,1}(end-5:end));
```

```
            ctl.vhold{ctl_count,1} =
str2double(ctl.comment{ctl_count,1}{1,2}(8:end));
            ctl.controlsig{ctl_count,1} =
ctl.comment{ctl_count,1}{1,4}(17:end);
            ctl_count = ctl_count + 1;
        else
            % Allocate Resonance Curve Data
            rc.vcov{rc_count,1} = seg2mat(d{i,1},3);
            rc.vcof{rc_count,1} = seg2mat(d{i,1},4);
            rc.mag{rc_count,1} = seg2mat(d{i,1},1);
            rc.phs{rc_count,1} = seg2mat(d{i,1},2);
            rc.name{rc_count,1} = files(i,1).name;
            rc_count = rc_count + 1;
        end
    end
   end
 clc;
 end
end
if ~exist('ctl','var')
   ctl = NaN;
end
if ~exist('rc','var')
    rc = NaN;
end
sens = regexp(foldername,'\','split');
testname = sens(end);
fprintf('Files Loaded Successfully!\n')
clearvars i rc_count ctl_count
% Filter
if nargin > 1
  if strcmp(StringIn,'filter') || strcmp(StringIn,'filt')
    Bf = ones(order/2,1)./(order/2);     %order is doubled when using
filtfilt
    Af = 1;
    for ctlnum = 1:length(ctl.vcov)
        fprintf('Filtering %d of %d...\n',ctlnum,length(ctl.vcov))
        ctl.vcov_f{ctlnum,1} = filtfilt(Bf,Af,ctl.vcov{ctlnum,1});
        ctl.vcof_f{ctlnum,1} = filtfilt(Bf,Af,ctl.vcof{ctlnum,1});
        ctl.vm_f{ctlnum,1} = filtfilt(Bf,Af,ctl.vm{ctlnum,1});
        clc
    end
    fprintf('Filtering Complete!\n')
  end
end
end
```